DIRECT GMSK MODULATION AT MICROWAVE FREQUENCIES

A Thesis Submitted to the College of
Graduate Studies and Research
in Partial Fulfilment of the Requirements
for the Degree of Doctor of Philosophy
in the Department of Electrical Engineering
University of Saskatchewan
Saskatoon

by

David Mathew Klymyshyn

Fall, 1998

UNIVERSITY OF SASKATCHEWAN

College of Graduate Studies and Research

SUMMARY OF DISSERTATION

Submitted in partial fulfillment

of the requirements for the

DEGREE OF DOCTOR OF PHILOSOPHY

by

David Mathew Klymyshyn

Department of Electrical Engineering
University of Saskatchewan

Fall 1998

Examining Committee:

Dr. W. Paulson	Dean/Associate Dean, Dean's Designate, Chair College of Graduate Studies and Research
Dr. T.S. Sidhu	Chair of Advisory Committee, Department of Electrical Engineering
Dr. S. Kumar	Supervisor, Department of Electrical Engineering
Dr. P. Pramanick	Department of Electrical Engineering
Dr. A.E. Krause	Department of Electrical Engineering
Dr. R.E. Pywell	Department of Physics and Engineering Physics

External Examiner:

Dr. R.H. Johnston
Department of Electrical and Computer Engineering
University of Calgary
2500 University Drive N.W.
Calgary, Alberta T2N 1N4

DIRECT GMSK MODULATION AT MICROWAVE FREQUENCIES

Congestion in the radio spectrum is forcing emerging high rate wireless communication systems into upper microwave and millimeterwave frequency bands, where transceiver hardware architectures are less mature. One way to realize a simple and elegant hardware solution for a microwave transmitter is to exploit the advantages of directly modulating the phase of the carrier signal.

A modulation method requiring continuous phase control of the carrier signal over the full 360 degree range is Gaussian Minimum Shift Keying (GMSK). Unfortunately, it is very difficult to design a microwave circuit to provide linear phase control of a carrier signal over the full 360 degree range using traditional methods. A novel method of obtaining continuous, linear phase modulation of a microwave carrier signal over the full 360 degree range is proposed. This method is based on controlling a phase shifter, at a subharmonic of the desired output carrier frequency, and then using a frequency multiplier to obtain the desired output frequency. The phase shifter is designed to be highly linear over a fraction of the full 360 range. The frequency multiplier is a nonlinear circuit that shifts the frequency by $\times N$. The subtle part of this nonlinear operation is that the multiplier also multiplies the instantaneous phase of the phase shifter output signal by $\times N$, thus expanding the linear phase shift range to the required 360 degrees. Using this nonlinear frequency multiplication principle, the modulator can readily be extended into the millimeterwave region.

A prototype circuit is designed and performance results are presented for this method of carrier phase modulation at 18 GHz. The prototype circuit is realized with very simple hardware, containing only a single microwave active device. An extension to the modulator involving phase locking or injection locking of a power oscillator is also suggested for obtaining higher power modulated output signals. In addition to direct continuous phase modulation, the proposed method is also suitable for a wide variety of transceiver applications, including phase synchronization of antenna and oscillator arrays, phased array antenna beam steering, indirect frequency modulation, and ultra-small carrier frequency translation.

PERMISSION TO USE

In presenting this thesis in partial fulfilment of the requirements for a Postgraduate degree from the University of Saskatchewan, I agree that the Libraries of this University may make it freely available for inspection. I further agree that permission for copying of this thesis in any manner, in whole or in part, for scholarly purposes may be granted by the professor or professors who supervised my thesis work or, in their absence, by the Head of the Department or the Dean of the College in which my thesis work was done. It is understood that any copying or publication or use of this thesis or parts thereof for financial gain shall not be allowed without my written permission. It is also understood that due recognition shall be given to me and to the University of Saskatchewan in any scholarly use which may be made of any material in my thesis.

Requests for permission to copy or to make other use of material in this thesis in whole or part should be addressed to:

Head of the Department of Electrical Engineering
University of Saskatchewan
Saskatoon, Saskatchewan, Canada
S7N 5A9

ACKNOWLEDGEMENTS

The author expresses his sincere gratitude to Professor Surinder Kumar for his valuable guidance and encouragement throughout the course of this research. Thanks also to the members of his advisory committee, Professors P. Pramanick, A. E. Krause, and R. E. Pywell for their assistance in preparing this thesis.

The University of Saskatchewan and Telecommunications Research Laboratories (TRLabs) are gratefully acknowledged for providing financial support for this research. The author also thanks the staff of TRLabs for their encouragement, support and guidance.

Special thanks is extended to the author's family for their encouragement and support and especially to his wife Sherry for her many sacrifices and endless patience.

ABSTRACT

As a result of congestion in the traditional microwave portions of the radio spectrum, new and emerging high rate wireless communication systems are migrating to the upper microwave and millimeter-wave frequency bands, where transceiver hardware architectures are less mature. For this reason, research into effective transmitter realizations at these frequencies is very timely. One way to realize an effective transmitter solution is to exploit the advantages of directly modulating the phase of a microwave carrier signal. Modulating the carrier phase directly, as opposed to the more traditional method of modulation at an IF frequency and use of multiple stages of up-conversion to reach the desired transmit frequency, results in a simple and elegant hardware solution for a microwave transmitter.

A modulation method requiring continuous phase control of the carrier signal over the full 360 degree range is Gaussian Minimum Shift Keying (GMSK). GMSK is a constant envelope continuous phase modulation method that has become popular recently, especially for mobile radio applications. Unfortunately, it is very difficult to design a microwave circuit to provide linear phase control of a carrier signal over the full 360 degree range using traditional methods. A novel method of obtaining continuous, linear phase modulation of a microwave or millimeter-wave carrier signal over the full 360 degree range is proposed. This method is based on controlling a phase shifter, at a subharmonic of the desired output carrier frequency, and then using a frequency multiplier to obtain the desired output frequency. The phase shifter is designed to be highly linear over a fraction of the full 360 range. The frequency multiplier is a nonlinear circuit which shifts the frequency by $\times N$. The subtle part of this nonlinear operation is that the multiplier also multiplies the instantaneous phase of the phase shifter output signal by $\times N$, thus expanding the linear phase shift range to the required 360 degrees. Using this nonlinear frequency multiplication principle, the modulator can readily be extended into the millimeter-wave region.

A prototype circuit is designed to verify this proposed method of carrier phase control at 18 GHz. The prototype circuit is realized with very simple hardware, containing only a single microwave active device. An extension to the modulator involving phase locking or injection locking of a power oscillator is also suggested for obtaining higher power modulated output signals. In addition to direct continuous phase modulation, the proposed method is also suitable for a wide variety of transceiver applications, including phase synchronization of antenna and oscillator arrays, phased array antenna beam steering, indirect frequency modulation, and ultra-small carrier frequency translation.

Performance results are presented for GMSK modulation of a carrier signal at 18 GHz. Excellent performance in realizing GMSK at 18 GHz is

obtained by employing Gaussian prefiltered phase control signals. The full GMSK phase control range of 360 degrees was exercized with less than 5 degrees of phase distortion in the modulated signal while maintaining the near constant envelope property desired for GMSK. The result of this performance is exceptional GMSK modulated signal characteristics at moderate data rates. The modulator provided an output level of -10 dBm at 18 GHz and good frequency selectivity as all undesired harmonics were maintained at < -30 dBc. The modulator was shown to be suitable for high frequency modulating signals and performed favourably at modulation frequencies as high as 300 MHz.

The results of this research are very encouraging and present an effective method of direct modulation that is very attractive for many applications emerging at upper microwave and millimeter-wave frequencies.

Table of Contents

List of Figures

List of Tables

ABBREVIATIONS

ACI	adjacent channel interference
ATM	asynchronous transfer mode
AM	amplitude modulation
BER	bit error rate
bps	bits per second
BPSK	binary phase shift keying
CPM	continuous phase modulation
CPFSK	continuous phase FSK
CV	capacitance versus voltage
CW	continuous wave
dB	decibel
dBc	decibels relative to carrier
dBm	decibels relative to 1 milliwatt
DC	direct current
EMI	electromagnetic interference
FET	field effect transistor
FM	frequency modulation
FSK	frequency shift keying
GaAs	gallium arsenide
GHz	gigahertz
GMSK	Gaussian minimum shift keying
GSM	Global System for Mobile
HPA	high power amplifier
Hz	Hertz
I/Q	inphase and quadrature components
IF	intermediate frequency

ILO	injection locked oscillator
IMD	intermodulation distortion
IPSVD	interdigitated planar Schottky varactor diodes
ISI	intersymbol interference
kbps	kilo bits per second
kHz	kilohertz
LMCS	local multipoint communication system
LO	local oscillator
LPF	lowpass filter
mA	milliamps
Mbps	mega bits per second
MESFET	metal semiconductor FET
MIC	microwave integrated circuit
mil.	0.001 inches
MHz	megahertz
MMIC	monolithic microwave integrated circuit
MSK	minimum shift keying
μs	microseconds
NBFM	narrowband frequency modulation
NRZ	non-return to zero
nH	nanohenries
ns	nanoseconds
Ω	Ohms
OQPSK	offset quadrature phase shift keying
pF	picofarads
PCS	Personal Communication Service
PLL	phase locked loop
PLO	phase locked oscillator
PM	phase modulation
PSK	phase shift keying

Q	quality factor
QPSK	quadrature phase shift keying
RF	radio frequency
SDH	synchronous digital hierarchy
SNR	signal to noise ratio
SRD	step recovery diode
STM	synchronous transport module
V	Volts
VCO	voltage controlled oscillator
WLAN	wireless local area network

1. INTRODUCTION

1.1 Background

Wireless communication methods have been in use for over 100 years [1]. Digital wireless communication, in one form or another, has been around since World War II and has been commercially available for the past quarter century [1].

Communicating digitally involves transmission of information represented by symbols rather than by analog waveforms. This method of communicating began over a century ago in the form of telegraphy, which employed the Morse Code for transmission of data. Transmission of analog signals such as audio and video in digital form was not possible until ways of sampling and coding of analog waveforms were pioneered by Nyquist and Shannon.

Wireless transmission of digital information is achieved in much the same way as wireless analog transmission. The amplitude, frequency, or phase of a sinusoidal carrier signal is modulated by the baseband information signal. In the case of digital communication, the baseband information signal is a sequence of discrete symbols rather than a continuous, time varying signal as in analog communication.

Military and space communication requirements drove early advancements in digital wireless technology and have paved the way for current commercial systems. The current explosive commercial growth is a result of the superior performance and flexibility of digital wireless communications, as compared to traditional analog wireless communication systems.

1.2 High Speed Digital Radio

There is an ever increasing demand for the ability to transfer data at high rates. One example of this is the growing popularity of the asynchronous transfer mode (ATM) of data transfer which is an efficient method for providing multimedia services such as voice, video, and data [2]. In ATM, digital data is assembled into fixed length packets. As the name indicates, ATM is an asynchronous protocol, and transmission of the packets is not synchronised to a system clock. These packets, however, are usually inserted into the synchronous framing structure of the Synchronous Digital Hierarchy (SDH) [3]. The lowest SDH rate for this purpose is Synchronous Transport Module level 1 (STM-1), a rate of 155.52 Mbps [3]. Because of the bandwidth requirement, most commercial ATM systems deployed to date, or in various stages of development, are optical fiber based systems [2]. Other current or emerging high data rate systems include Wireless Local Area Networks (WLANs) and Local Multipoint Communication Systems (LMCS).

Radio systems have certain advantages over fiber based systems. These include portability, rapid deployment, and ease of installation, in areas where fiber installation is often impractical and expensive [2]. Radio systems also offer the possibility of mobility, which is not an option with fiber based systems. Unfortunately, the radio spectrum is becoming increasingly congested in the traditional communication bands. As a result, future high capacity digital radio systems are being forced into the upper microwave and millimeter-wave bands, where existing transceiver design technology is less mature. Recent advances, however, in solid state device technology at these frequencies are making cost effective, high rate commercial transceiver circuits feasible [4]. High performance and cost effective radio transmitter solutions in these frequency bands are required in the design of future high capacity digital radio systems.

1.3 Direct Modulation

Direct digital modulation at the transmit frequency is a method by which the amplitude, phase, or frequency of a sinusoidal carrier is modulated directly by the baseband information sequence, as opposed to the more conventional method of modulation at an intermediate frequency (IF) and upconversion to the desired transmit frequency. Direct modulation at microwave frequency is an attractive option for reducing the cost and complexity of the transmitter, as it removes the requirement for IF, upconversion, and filtering circuitry. Also, if the carrier produced by a microwave power device is directly modulated at the desired transmit level, the requirement for a high power amplifier (HPA) as the final stage in the transmitter is removed.

Most digital modulation methods require encoding of baseband symbol information in the phase of the carrier. Some methods rely only on carrier phase modulation, while others encode the baseband data as a combination of carrier phase and amplitude modulation. The ability to accurately control the phase of the carrier signal over the full 360 degree range is a fundamental requirement of direct modulation. A simple and effective hardware architecture for performing direct phase modulation is very attractive for future modulator applications.

One modulation method requiring continuous carrier phase control is Gaussian Minimum Shift Keying (GMSK). GMSK is a relatively spectrally efficient modulation method [5] that has received considerable attention recently. It has been chosen as the modulation method for the Global System for Mobile (GSM) cellular system as well as the Digital Cordless Telephone (DCS1800) Personal Communication Service (PCS) standard [6]. An important characteristic of this modulation is its suitability for direct high power generation using a microwave device [7]. Also, the nearly constant envelope property of the GMSK modulated signal makes it fairly insensitive to nonlinearity in the transmitter [8]. This results in inexpensive, compact,

and highly power efficient transmitter designs. GMSK modulation also has the advantage that it may be demodulated using coherent [5] or noncoherent [9][10] detection methods. This leads to a simpler receiver structure. A brief description of GMSK modulation is presented in the next section.

1.4 Gaussian Minimum Shift Keying

Minimum shift keying (MSK) is a special case in the family of constant envelope continuous phase modulation (CPM) signals [11] in which the carrier phase is modulated over the full 360 degree range. MSK is equivalent to continuous phase frequency shift keying (CPFSK) with a modulation index of 0.5. Being a frequency modulated (FM) signal, the MSK modulated signal has a constant envelope. Thus, the modulated signal is fairly insensitive to transceiver nonlinearity which gives rise to modulated signal amplitude and phase distortion. Other desirable properties of MSK are its relatively compact spectral main lobe and the ability to detect the signal using coherent or noncoherent means.

The spectral side lobes of the MSK modulated signal roll off rather slowly. This wideband spectral characteristic is a result of the sharp phase transitions in the modulated signal. Thus, it is not a feasible modulation method in the radio environment, where out of band radiation and adjacent channel interference are strictly controlled. A premodulation Gaussian lowpass filter is generally used to smooth the sharp phase transitions and filter the out of band power.

1.4.1 Traditional Modulator Architectures

The easiest way to generate GMSK is to modulate a voltage controlled oscillator (VCO) with the incoming serial data stream, correctly scaled in amplitude for a modulation index of 0.5 and filtered by the Gaussian premodulation filter, as shown in Figure 1.1. This method is well suited for

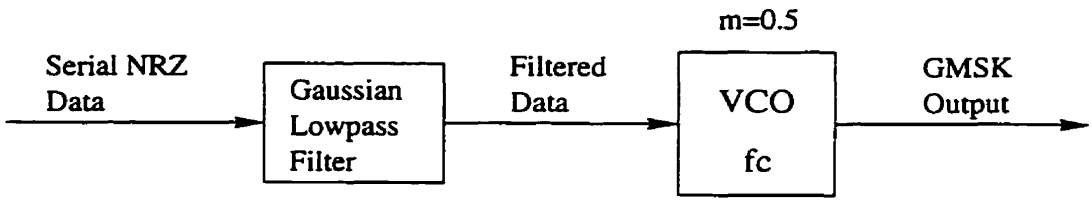


Figure 1.1 Traditional serial GMSK modulator using a VCO.

direct modulation, as the VCO output frequency can be the desired transmit frequency. In practice, however, frequency drift in the VCO makes this method impractical for most microwave radio applications.

Another common method of generating MSK at low frequencies is to modulate quadrature carriers, which is equivalent to offset quadrature phase shift keying (OQPSK) modulation with sinusoidal baseband pulse shaping [12]. This parallel generation method, shown in Figure 1.2, produces an output modulated signal which is stable in frequency. This method of MSK generation, however, is less appropriate than the serial generation method for high data rates and high carrier frequencies due to difficulties in maintaining I/Q amplitude and phase balance [13]. It is also more difficult to apply baseband Gaussian filtering, as a result of the separation into I and Q channels.

A method of direct GMSK modulation providing a frequency stable modulated output signal with simple and realizable hardware at microwave or millimeter-wave frequency is very attractive for future high capacity radio systems.

1.5 Literature Review

There is considerable literature on the two classic methods of generating MSK or GMSK described above [5][12][13][14][15][16]. However, very few methods specific to direct GMSK modulator architectures suitable for use at

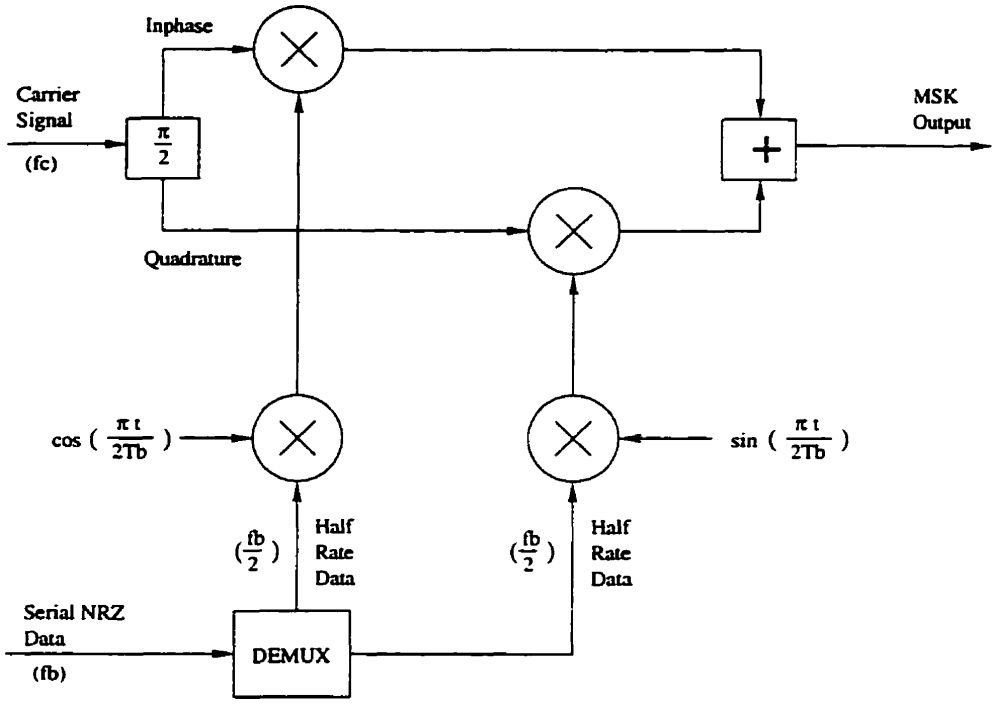


Figure 1.2 Parallel MSK modulator using quadrature carriers.

microwave or millimeter-wave frequencies have been reported.

Murota and Hirade [5] proposed a direct GMSK modulation method whereby a carrier is modulated using a $\pi/2$ shift binary phase shift keying (BPSK) modulator. The signal is then input to a phase locked loop (PLL) with loop response designed to convert the $\pi/2$ shift BPSK signal to a GMSK signal by shaping the modulated carrier signal phase.

Ziemer and Ryan [13] proposed a passband spectral conversion method. In this method, a stable directly modulated MSK signal was obtained by first BPSK modulating the carrier at a lower than desired output frequency, $f_o - \frac{1}{4T_b}$, and then converting the BPSK spectrum into an equivalent MSK spectrum at f_o by passing the signal through a $\sin(x)/x$ shaped bandpass conversion filter centred at a frequency of $f_o + \frac{1}{4T_b}$. It is difficult to control the bandpass conversion filter response and centre frequency at microwave or millimeter-wave frequencies. Also, there is no conversion filter representation

to implement the Gaussian filtering required for GMSK.

Kumar [7] proposed a direct FM technique for realizing GMSK in which frequency stability was achieved by phase locking a VCO to the carrier signal recovered from the GMSK modulated output signal. This technique is attractive, but results in complicated hardware that may be difficult to implement at microwave or millimeter-wave frequencies.

From the literature review, it is evident that not much has been reported on direct GMSK modulator architectures that result in simple and realizable hardware architectures at microwave and millimeter-wave frequencies. GMSK is one modulation method that could certainly benefit from effective realization of full 360 degree carrier phase control capability at these frequencies. With the current explosion in proposed high data rate communication systems at these frequencies, it is apparent that research in this area is quite timely.

1.6 Research Objectives

The main objectives of the research are summarised as follows:

- Devise a suitable hardware architecture for direct GMSK modulation at microwave frequency.

- Implement the proposed hardware architecture using realistic microwave circuitry.

- Evaluate the performance of the circuitry in realizing direct GMSK modulation at microwave frequency.

1.7 Thesis Organization

This thesis is organized into seven chapters. In Chapter 2, a brief overview of GMSK modulation and direct GMSK modulation techniques is presented.

Several direct GMSK architectures are considered and the most promising architecture, based on a fractional CPFSK modulator with frequency/phase multiplier, is chosen for implementation.

In Chapter 3, the direct GMSK modulator architecture is discussed in detail. An extension of the direct GMSK modulator option is proposed which combines the fractional CPFSK modulator with frequency/phase multiplier architecture with a high power phase locked oscillator (PLO). Simulation results for this method are presented.

In Chapter 4, design considerations and the theoretical relationships required to realize the direct GMSK modulator at microwave frequency are presented. These relationships are expanded in Chapter 5, and detailed microwave circuit designs and simulation results to be used as comparison for later measured results are presented.

In Chapter 6, details of the GMSK modulator fabrication are discussed and the measured modulator performance for direct GMSK modulation at microwave frequency is presented and compared to the simulation results of Chapter 5.

In Chapter 7, conclusions of this research are presented and future research directives are suggested.

2. DIRECT GMSK MODULATION METHODS

In this chapter, the characteristics of GMSK modulation that make it a suitable modulation method in the radio environment are reviewed. Potential direct GMSK modulator architectures are described, including some published direct GMSK modulation architectures, and some new architectures. A novel GMSK modulator architecture is proposed for implementation, and this architecture is described in detail in Chapter 3.

2.1 GMSK Modulation Characteristics

In communication transceivers, modulated signal distortion results due to nonlinearities in the power amplifiers [17]. Popular modulation methods with signal envelopes having varying amplitude are very sensitive to power amplifier nonlinearity, which causes intermodulation distortion (IMD) in the output signal [8]. Another impairment due to nonlinearity is the spreading in frequency of the filtered modulated signal spectrum. This is known as spectral spreading [8]. One way to reduce these nonlinear distortion effects is to operate the power amplifier significantly below output power saturation, thereby avoiding the highly nonlinear portion of the complex gain characteristic [8]. This, however, results in low amplifier power efficiency. Operating transmitter power amplifiers at low efficiency does not usually result in inexpensive and compact designs for mobile transceivers as large batteries are required to supply excess power, while large heat sinks are required to dissipate this power.

Minimum shift keying (MSK) is an example of a constant envelope mod-

ulation [11] in which the carrier phase is modulated continuously over the full 360 degree range. MSK is equivalent to continuous phase frequency shift keying (CPFSK) with a modulation index (m) of 0.5. Because it is an FM signal, the unfiltered MSK modulated signal has a constant envelope. Thus, the MSK modulated signal is fairly insensitive to transceiver nonlinearity which causes distortion with varying envelope, linear modulation methods. Therefore, it is possible to amplify the MSK modulated signal using a power efficient, nonlinear amplifier. In addition to power efficient transmitter operation, very little power is required at the receiver to obtain acceptable demodulator performance [16]. Both of these factors make MSK a power efficient modulation method. Other desirable properties of MSK are its relatively compact spectrum and coherent detection capability [5]. Also, as MSK is an FM signal, it is inherently robust in a fading environment, which is experienced in mobile communications.

In general, a CPM signal is represented as

$$s(t) = A\cos[\omega_c t + \phi(t)], \tag{2.1}$$

where A represents the constant envelope of the modulated signal, ω_c is the carrier frequency, and $\phi(t)$ is the excess phase of the modulated carrier as a continuous function of time. In the case of MSK, $\phi(t)$ is controlled continuously during the modulating signal bit interval, $nT_b \leq t \leq (n+1)T_b$. The excess phase of the MSK modulated signal with modulation index of 0.5, in the interval $nT_b \leq t \leq (n+1)T_b$, is

$$\phi(t) = \phi_n + \frac{b_n \pi (t - nT_b)}{2T_b}, \tag{2.2}$$

where T_b is the bit interval, ϕ_n is the phase at the start of the bit, and $b_n = \pm 1$ represents the baseband binary modulation signal.

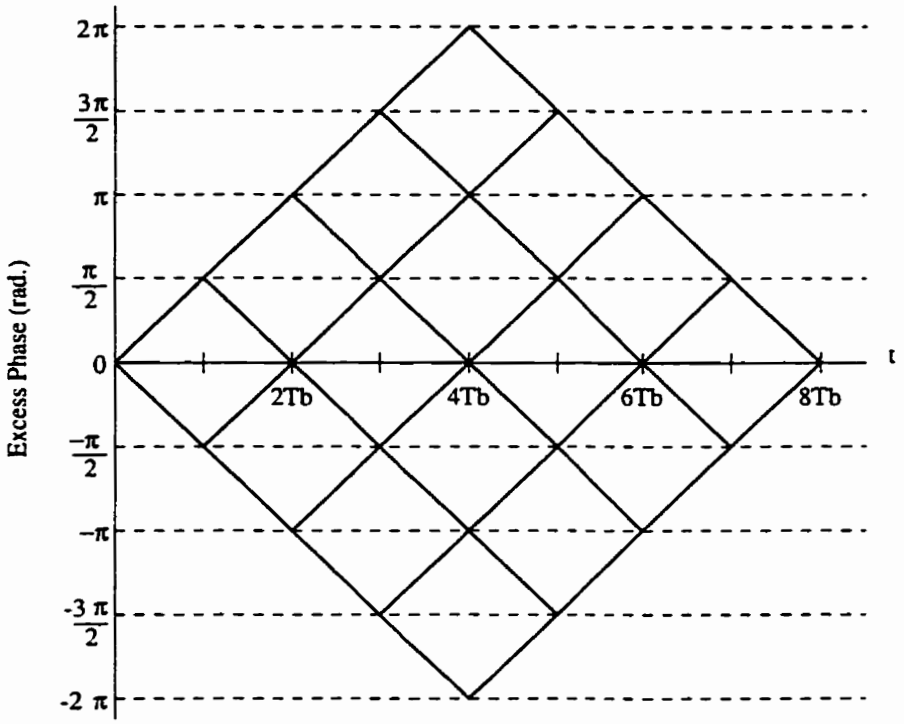


Figure 2.1 MSK modulated signal excess phase trellis.

From Equation 2.2, it is apparent that the modulated carrier phase will change, continuously, by $\pm\pi/2$ radians over the bit interval $nT_b \leq t \leq (n+1)T_b$. Therefore, Equation 2.1 for the MSK modulated signal in the interval $nT_b \leq t \leq (n+1)T_b$ may be written as

$$s_n(t) = A\cos\left[\omega_c t + \frac{b_n \pi t}{2T_b} + \phi_n\right]. \tag{2.3}$$

The modulated signal excess phase as a function of time is conveniently represented using a trellis diagram, as shown in Figure 2.1. The trellis diagram shows all possible paths in the output excess phase trajectory as a function of time.

As seen from Equation 2.3, the excess phase of the carrier is directly modulated by the incoming serial bit stream. Therefore, this method of MSK generation is known as a serial generation method. Equation 2.3 can

also be written as

$$s_n(t) = A\cos\left[2\pi\left(f_c + \frac{b_n}{4T_b}\right)t + \phi_n\right]. \tag{2.4}$$

Equation 2.4 represents a CPFSK modulated signal with mark and space tones of

$$f_+ = f_c + \frac{1}{4T_b}, \tag{2.5}$$

$$f_- = f_c - \frac{1}{4T_b}, \tag{2.6}$$

and a frequency deviation of

$$\Delta f = f_+ - f_- = \frac{1}{2T_b}, \tag{2.7}$$

or one half of the bit rate. This is the minimum frequency separation that maintains orthogonality between the signals [14] and allows the MSK modulated signal to be coherently demodulated. This is the origin of the name "Minimum Shift Keying".

The easiest way to generate MSK serially is to modulate a voltage controlled oscillator (VCO) with the incoming serial data stream, correctly scaled in amplitude for a modulation index of 0.5. In practice, frequency drift in the VCO makes this method impractical for most radio applications.

Alternatively, a parallel form for MSK modulation can be derived which is equivalent to offset quadrature phase shift keying (OQPSK) modulation with sinusoidal baseband pulse shaping [12]. The equivalence of OQPSK with sinusoidal baseband pulse shaping to MSK can be demonstrated by applying trigonometric identities to Equation 2.3, with $\phi_n = 0$, to obtain [12]

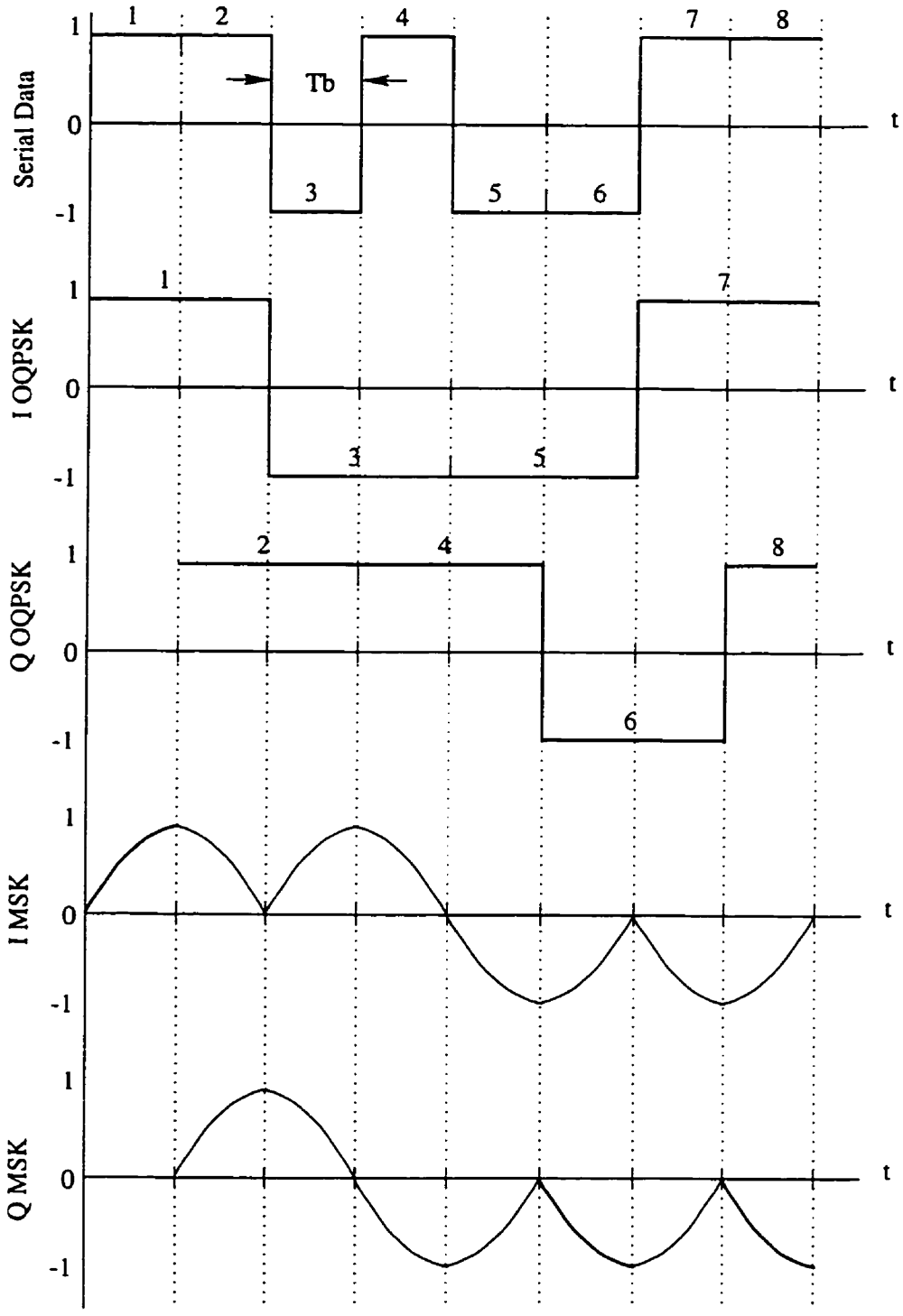


Figure 2.2 I and Q waveforms for OQPSK and OQPSK with sinusoidal baseband pulse shaping (MSK).

$$s_n(t) = A\left[p_n \cos\left(\frac{\pi t}{2T_b}\right)\cos\omega_c t + q_n \sin\left(\frac{\pi t}{2T_b}\right)\sin\omega_c t\right], \qquad (2.8)$$

where $p_n = \pm 1$ and $q_n = \pm 1$ represent consecutive bits in the serial bit stream. This parallel representation is equivalent to the serial representation of Equation 2.3, with $b_n = p_n q_n$ controlling either an increase or decrease in excess phase. This implies that the input bit sequence is differentially encoded for the parallel representation, with $p_n = q_n$ representing an increase in carrier excess phase and $p_n \neq q_n$ representing a decrease in carrier excess phase.

Figure 2.2 shows the decomposition of the parallel MSK modulating signal into equivalent baseband I and Q waveforms for a series of input bits. As the quadrature carriers are stable in frequency, the modulated output signal is also stable in frequency. This method of MSK generation, however, is less appropriate than serial generation for high data rates and high carrier frequencies due to difficulties in maintaining I/Q amplitude and phase balance [13].

The MSK modulated signal single sided power spectral density is shown in Figure 2.3. As seen in Figure 2.3, the main lobe of the MSK modulated signal is quite compact, with 90% of the signal power within a bandwidth of $0.78R_b$ [5]. The spectral side lobes of the MSK modulated signal, however, roll off rather slowly. As a result, MSK is not a feasible modulation method in the radio environment, where out of band radiation and adjacent channel interference are strictly controlled. The wideband nature of the MSK modulated signal results from the sharp phase transitions, as indicated in the trellis diagram of Figure 2.1. It is desirable to filter these sharp phase transitions in such a way as to reduce the spectral sidelobe levels, while maintaining the desirable properties of MSK, namely, constant envelope and coherent detection capability. A Gaussian premodulation lowpass filter [18] is gener-

ally used with MSK at baseband for smoothing the sharp phase transitions and limiting the out of band power. The Gaussian filter response is appropriate for this purpose as it maintains the constant envelope property and preserves the pattern-averaged phase-transition trajectory, enabling coherent detection [5].

The ideal Gaussian lowpass filter response [18], $H(j\omega)$, has constant group delay and exponentially decaying amplitude response

$$|H(j\omega T_b)| = \exp\left(-\frac{\ln 2}{2}\left(\frac{\omega T_b}{2\pi BT_b}\right)^2\right), \tag{2.9}$$

where T_b is the input data bit period and BT_b is the lowpass filter 3 dB bandwidth normalized to the bit period. The amplitude response of the Gaussian lowpass filter for various values of BT_b is shown in Figure 2.4.

The power spectral density for MSK and GMSK, with various Gaussian filter 3 dB bandwidths normalized to the bit rate. BT_b, is shown in Figure 2.3. Figure 2.3 demonstrates the effect of the Gaussian premodulation filter on reducing the out of band power in the modulated output spectrum. It is apparent from comparing Figures 2.3 and 2.4 that the Gaussian filter response applied at baseband does not transfer linearly to the modulated output spectrum. This is because GMSK is a nonlinear modulation. By using a Gaussian premodulation filter with $BT_b = 0.2$, GMSK can approach 1.9 bps/Hz [5] spectral efficiency, when the bandwidth is based on 90% of the modulated output power.

Use of the Gaussian premodulation filter to restrict the output spectrum does not come without a price, as it causes intersymbol interference (ISI) in the modulated signal. This effect is a result of the carrier excess phase trajectory being restricted by the Gaussian filter to less than $\pi/2$ radians over the bit duration, at the phase transition points in the trajectory. This essentially violates the minimum tone spacing constraint of MSK, causing

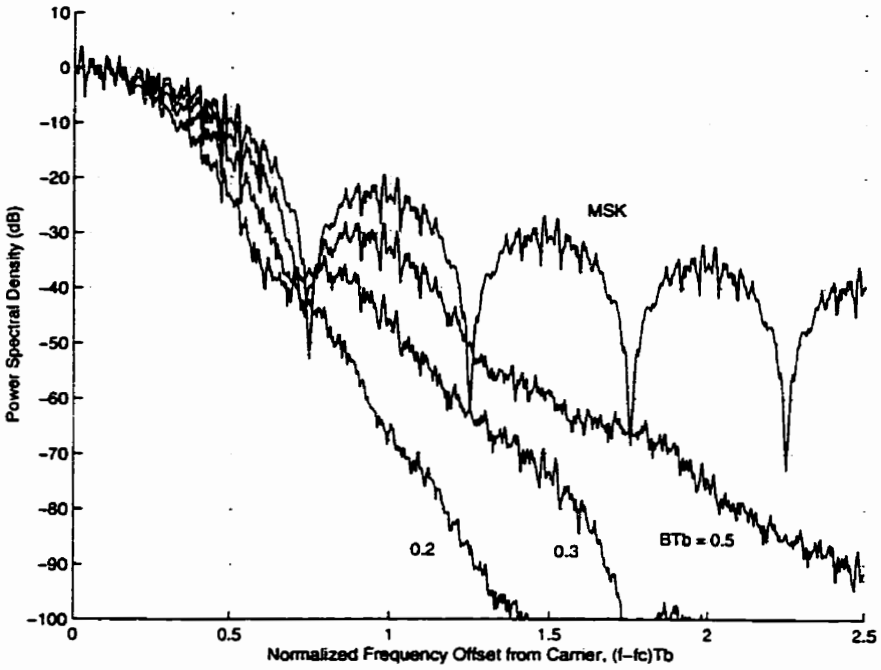


Figure 2.3 Power spectral density of MSK and GMSK for various values of BT_b.

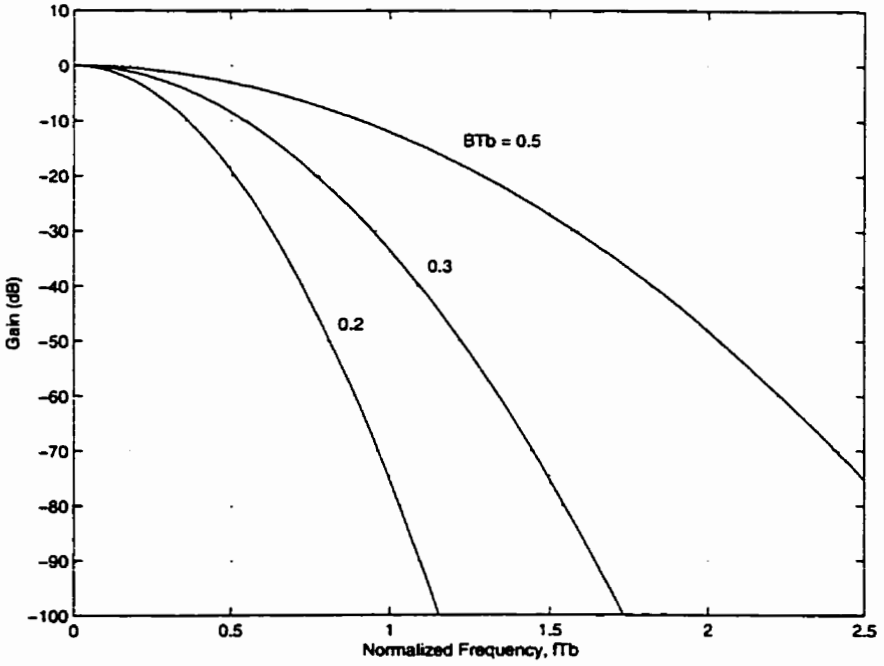


Figure 2.4 Gaussian filter amplitude response for various values of BT_b.

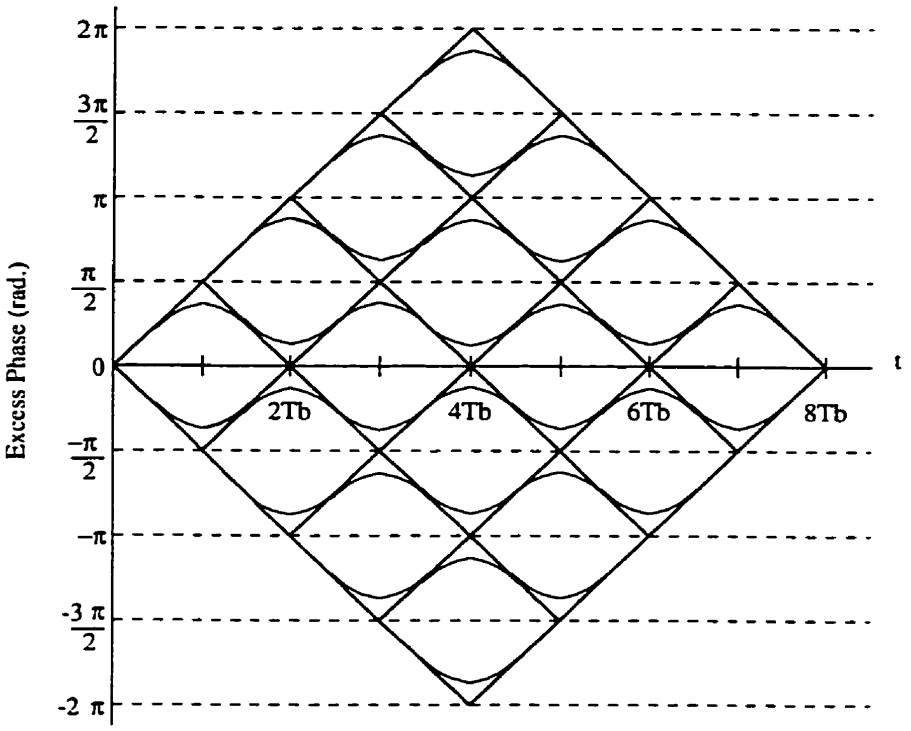


Figure 2.5 Effect of Gaussian filtering on the modulated signal excess phase trellis.

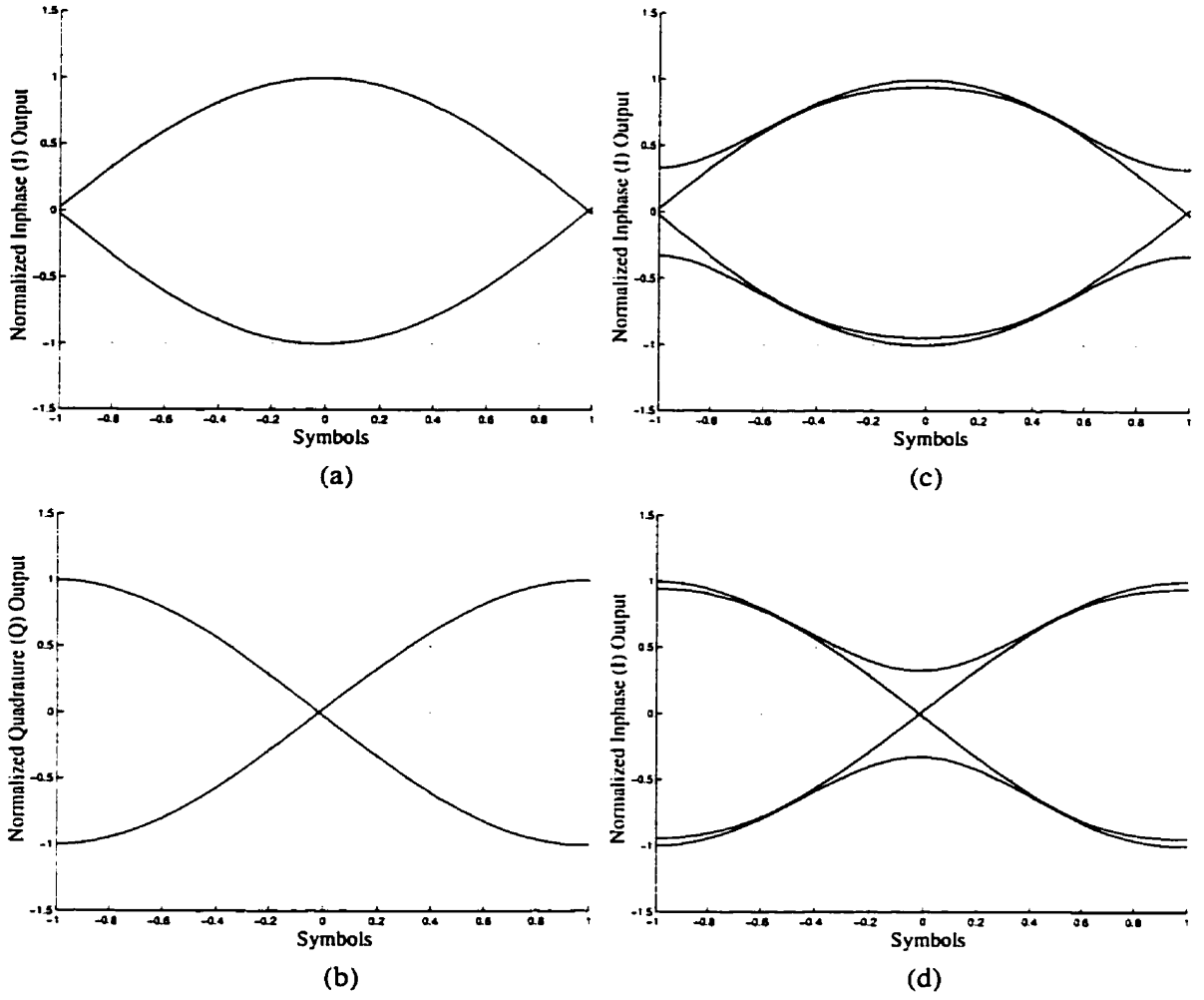


Figure 2.6 Ideal coherent demodulation of MSK and 0.5 GMSK modulated signal: (a) Inphase Eye (MSK); (b) Quadrature Eye (MSK); (c) Inphase Eye (0.5 GMSK); (d) Quadrature Eye (0.5 GMSK).

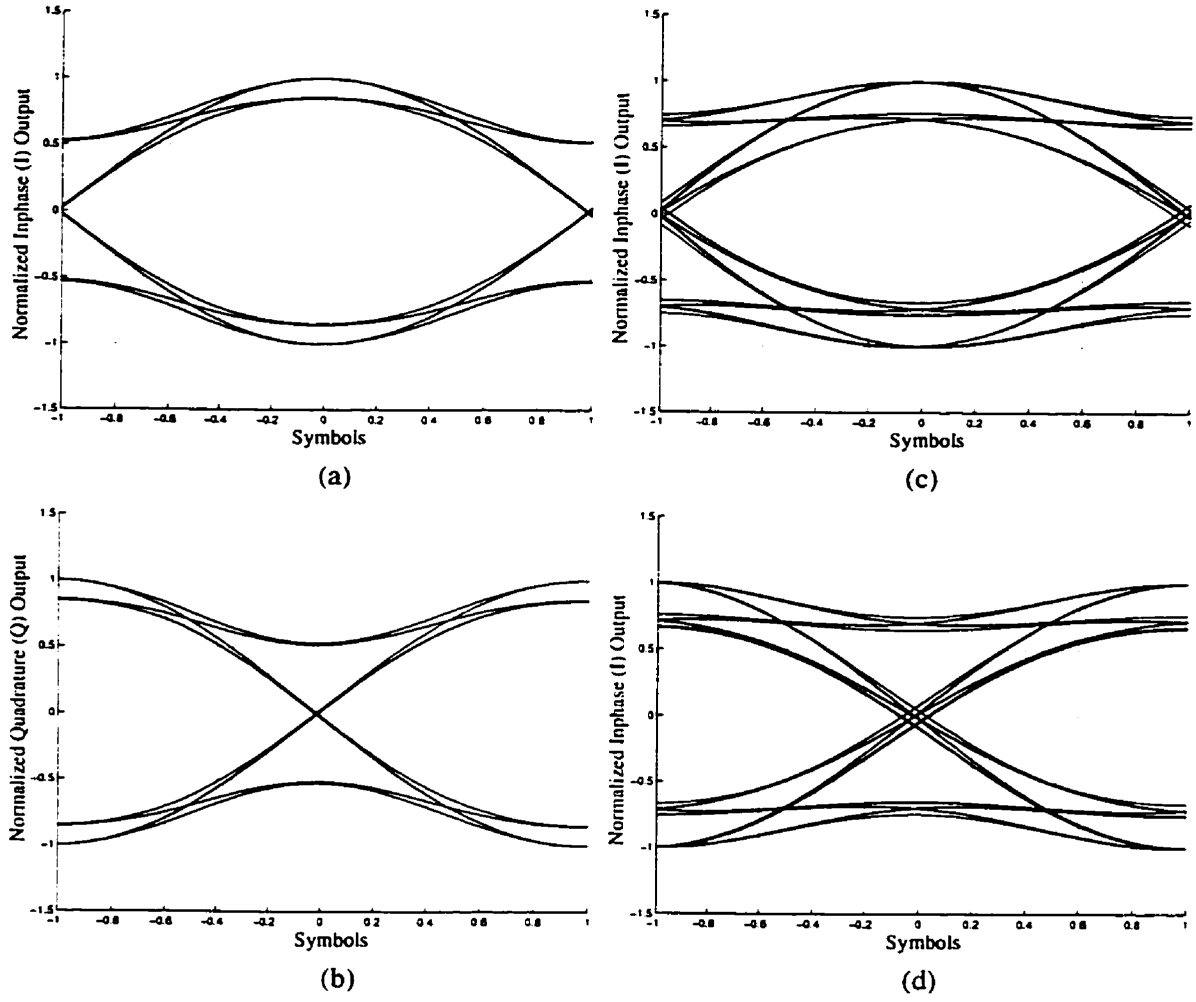


Figure 2.7 Ideal coherent demodulation of 0.3 GMSK and 0.2 GMSK modulated signal: (a) Inphase Eye (0.3 GMSK); (b) Quadrature Eye (0.3 GMSK); (c) Inphase Eye (0.2 GMSK); (d) Quadrature Eye (0.2 GMSK).

the ISI. The effect of Gaussian filtering on the carrier excess phase at the phase transitions is demonstrated by the trellis diagram of Figure 2.5.

The violation in the minimum tone spacing constraint caused by the Gaussian filter degrades, but does not necessarily prohibit, coherent demodulation. This is because the pattern-averaged phase transition trajectory, as shown in Figure 2.5, does not deviate from that of simple MSK, as shown in Figure 2.1. Figures 2.6 and 2.7 show the ideal coherently demodulated in-phase (I) and quadrature (Q) "eye" diagrams for various values of BT_b, where the symbol period, T_s, equals T_b if the I and Q channels are sampled synchronously at a rate of f_b. The increased ISI with decreasing BT_b value, evident in Figures 2.6 and 2.7, does not result in significant degradation in demodulator bit error rate (BER) performance if the demodulated symbols are sampled synchronously at $T_s/2$. If the signal is demodulated coherently as OQPSK, $T_s = 2T_b$. The I and Q channels are sampled at the peaks of the eye openings, at a rate of $f_b/2$, using inverted bi-phase clocks. With OQPSK demodulation, the required increase in received signal to noise ratio for $BT_b = 0.25$ is only about 1 dB, to achieve comparable BER performance to MSK for BER $> 10^{-5}$ [5].

This discussion has shown that GMSK is a good overall modulation method, with reasonable spectral efficiency and high power efficiency. The next section discusses the realization of direct GMSK as a simple and inexpensive hardware solution.

2.2 Direct GMSK Architectures

This section describes some potential direct GMSK hardware architectures for use at microwave or millimeter-wave frequency. A novel architecture is proposed for implementation.

2.2.1 GMSK Generation using FM with Carrier Recovery

The classic method of GMSK generation using a direct FM modulator with premodulation Gaussian baseband filtering was described in Chapter 1. The problem with this method is that frequency drift in the VCO makes it impractical for most radio applications, where frequency stability in the radio channel is critical. Kumar [7] proposed a method of feedback control to stabilize the VCO output frequency.

In this method, the VCO is directly modulated by the Gaussian prefiltered baseband information signal, combined with a DC error signal for frequency tracking. The DC error signal is the output of a phase detector measuring the phase difference between a frequency stable reference signal and the recovered carrier signal from the GMSK modulated output. The GMSK modulated output signal is divided down in frequency and passed through a nonlinearity which produces a signal with a modulation index $m = 1.0$, containing a CW carrier component. This carrier component is recovered and fed back to the phase detector.

This method is promising, but the carrier recovery circuitry is not trivial, and leads to fairly complicated hardware which could be difficult to implement at microwave or millimeter-wave frequency. Therefore, a simpler hardware solution is desirable.

2.2.2 GMSK Generation from PSK

This architecture involves using phase shift keying (PSK) to modulate a CW carrier and then converting the PSK modulated signal to an MSK or GMSK modulated signal by use of appropriate filtering. The advantage of this architecture is that frequency stable direct modulation using PSK is quite simple to do. The disadvantage is that the conversion filter likely provides

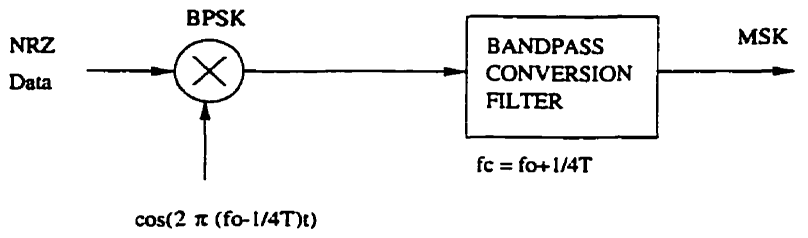


Figure 2.8 Direct MSK modulator with spectral conversion filter [13].

an approximation for the desired modulated output signal characteristics, as it is difficult to convert from a signal with discrete output phase changes, to one that changes phase continuously over the bit interval.

BPSK with Spectral Conversion

In Ziemer and Ryan [13], a stable directly modulated MSK signal was obtained by first BPSK modulating the carrier, at $f_o - \frac{1}{4T_b}$, and then converting the BPSK spectrum into an MSK spectrum at f_o by passing the signal through a $\sin(x)/x$ shaped bandpass conversion filter centred at $f_o + \frac{1}{4T_b}$. This method of serial generation, shown in Figure 2.8, is attractive since the modulator is memoryless and the conversion filter is realizable [13]. It is, however, difficult to implement at microwave and millimeter-wave frequencies, where accurate control of the bandpass conversion filter response and centre frequency is difficult. Also, there is no conversion filter representation to implement the Gaussian filtering required for GMSK, so this filtering would have to be done separately on the MSK signal after conversion.

Murota and Hirade [5] proposed a different spectral conversion method using a PLL to convert from BPSK to MSK and also provide Gaussian filtering. This method is shown in Figure 2.9.

This method does not employ an $f_o \pm \frac{1}{4T_b}$ frequency shift and is centred at f_o by the PLL. It requires a more complicated BPSK modulator with memory of the previous phase state, namely a $\pi/2$ shift BPSK modulator, on

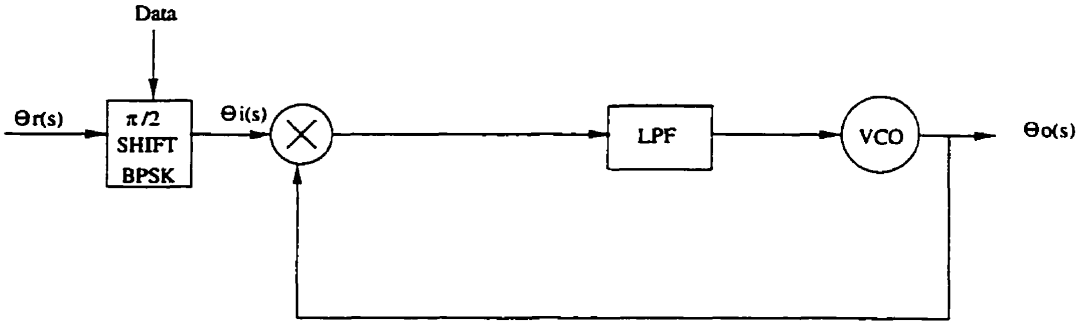


Figure 2.9 Direct GMSK modulator using a PLL [5].

the input rather than the simple BPSK modulator used in [13]. The $\pi/2$ shift BPSK modulator provides a phase change of $\pm\pi/2$ radians every bit, with memory of the carrier phase of the previous bit. The step change in phase error between the BPSK input signal and the VCO output signal of $\pm\pi/2$ radians at the phase detector output is filtered by the PLL loop response. The loop response is designed to approximate the Gaussian response, and filter the VCO control signal to provide a GMSK modulated output signal. This method is attractive, but becomes more complicated with the requirement of the $\pi/2$ shift BPSK modulator, as opposed to the simple BPSK modulator. A $\pi/2$ shift BPSK modulator requires a $\pi/2$ radian phase shift every bit, which can be realized using a combination BPSK modulator, 90 degree power divider, and a switch. It can also be realized as a full quadrature modulator. A modulator resulting in a simpler hardware solution would be desirable.

Other GMSK transmitter architectures using standard BPSK modulation of a carrier and a PLL were investigated. A BPSK modulator is more attractive to implement then the more complicated $\pi/2$ shift BPSK modulator. If the PLL could be designed to facilitate tracking of a stable reference signal, perform BPSK to MSK conversion on the modulated signal spectrum, and provide a Gaussian filter response to smooth the sharp MSK phase transitions and limit the out of band power, this would be a very attractive hardware architecture.

The problem that arises with the use of a simple BPSK modulator and

a PLL is in conversion to the MSK signal. This architecture is based on the fact that the output excess phase is the integration of phase detector output phase error as a result of BPSK modulation. Unfortunately, the loop cannot distinguish desired phase error from phase error caused by loop imperfections. That is, the loop integrates this undesired phase error as well as the intended phase error and eventually begins to deviate significantly from the path averaged excess phase trajectory, and thus cannot be coherently demodulated [5]. The most significant loop imperfection is the phase detector nonlinearity in sinusoidal type phase detectors. The sinusoidal nonlinearity in the BPSK type of modulator architecture is unavoidable, as the phase detector is comparing a constant phase input signal to a feedback signal which varies by $\pi/2$ radians over the bit period. Therefore, this method of direct GMSK modulation was abandoned.

2.2.3 MSK Generation using Indirect FM

An FM signal can be generated directly by modulating the frequency control input of a VCO with the baseband signal. It is also well known that FM can be generated indirectly from phase modulation (PM) [19][20], by integrating the baseband signal and using this signal to phase modulate a CW carrier.

The problem of integration error prevalent in the BPSK PLL architectures can be alleviated by restricting the function of the PLL to reference tracking and Gaussian filtering, and moving the integration function outside of the PLL.

One way of moving the integration function outside of the PLL is to integrate the input data signal at baseband and inject this AC modulation signal into the baseband portion of the PLL, while using an unmodulated carrier as the reference. This method, shown in Figure 2.10, is a type of indirect FM [19] in which the output frequency is proportional to the derivative of

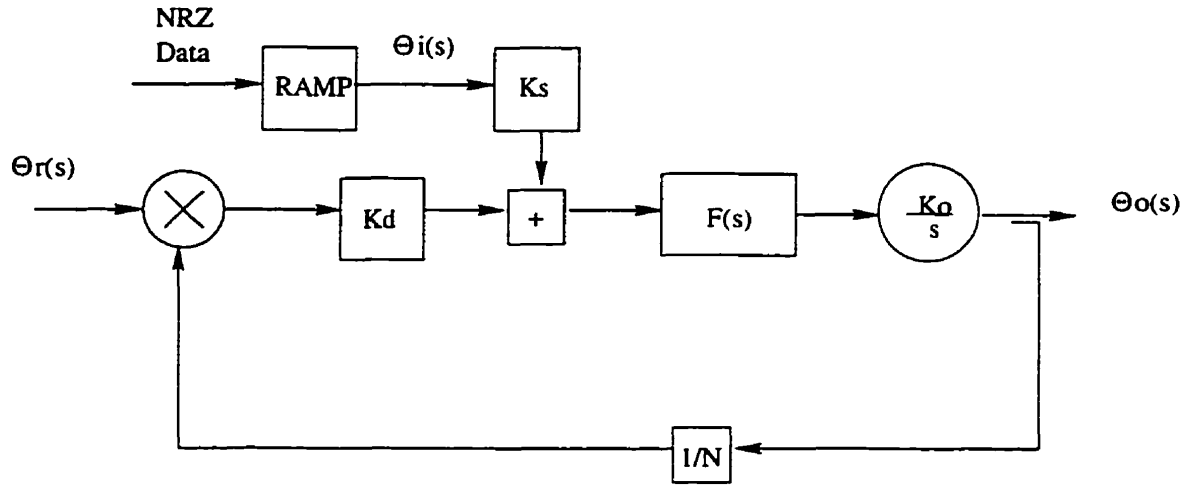


Figure 2.10 Indirect GMSK modulation using a PLL.

the modulating signal and is popular for low frequency FM modulation.

One problem with this method arises in the use of a sinusoidal phase detector, which is invariably the case at microwave frequencies. As with the BPSK architectures, the phase detector is comparing a constant phase reference signal with an output signal whose excess phase trajectory varies over the full 2π range. Therefore, this method requires a phase detector that is linear over the full 2π range. Such a phase detector is difficult to realize at microwave frequencies.

Another concern with indirect FM is in the handling of phase wrapping at the $\pm\pi$ radian boundary in the excess phase plane. In practical circuits, integration values cannot be unrestricted and must be constrained to within $\pm\pi$ radians. This involves subtraction of 2π radians at this boundary and could cause phase discontinuities in the loop if not handled properly.

The problem of the nonlinear phase detector can be overcome by integrating the baseband input data and linearly modulating the phase of the reference signal, rather than injecting the integrated baseband signal directly into the PLL. With baseband prefiltering, this architecture is suitable for GMSK modulation without the PLL on the output, provided that the phase

modulator is capable of full 360 degree phase control of the carrier signal. The next chapter proposes an alternative method of generating indirect FM, using a full range CPM modulator based on a fractional CPFSK modulator with a frequency/phase multiplier. This is a novel architecture resulting in a simple microwave hardware solution.

2.3 Summary

A number of architectures for achieving direct microwave GMSK modulation have been investigated. Kumar's method may be difficult to implement at upper microwave and millimeter-wave frequencies. The method of Ziemer and Ryan [13] is also difficult to implement at microwave frequencies and is more appropriate for MSK than GMSK. The method of Murota and Hirade [5] is better, but requires a more complicated $\pi/2$ shift BPSK modulator which is difficult to implement at microwave frequencies, and requires an approximation for the GMSK spectral conversion characteristics.

Methods employing input BPSK modulation and PLL integration are not appropriate at microwave frequencies due to the tendency of these architectures to deviate significantly from the desired output excess phase trajectory, as a result of phase detector error.

The method of indirect FM by injecting the modulation signal into the PLL suffers at microwave frequencies from the unavailability of a linear phase detection device. Therefore, this method is also not feasible for microwave implementation.

The most promising architecture for microwave implementation is a fractional CPFSK modulator with a frequency/phase multiplier. This architecture could be combined with a power amplifier, PLL, or injection locked oscillator (ILO) on the output if higher output levels are required. This is a novel architecture leading to a simple and realizable microwave implementa-

tion. This architecture is described in detail in Chapter 3 and is the focus of the remainder of the thesis.

3. DIRECT GMSK MODULATOR

This chapter presents the proposed direct GMSK modulator in detail. The proposed modulator is based on realization of a CPM modulator, with carrier phase control over the full 360 degree range. This basic modulator can be used to realize low level direct GMSK modulation at microwave or millimeter-wave frequencies, with Gaussian prefiltering. An extension is presented for adding a PLL to the output of the modulator, to provide higher output levels and also provide the Gaussian filtering, as an option to prefiltering.

3.1 Fractional CPFSK with Multiplier

A serial MSK generation architecture resulting in simple microwave hardware is realized using a CPM modulator to control the phase of a carrier signal. To realize MSK as CPM, the baseband binary signal must be integrated before phase modulation. Also, the CPM modulator must be capable of providing full 360 degree linear control of the carrier signal phase. This is very difficult to achieve in practice, although attempts to realize large range linear phase shifters have been made for quite some time [21]. Most successful microwave linear phase shifters are based on a single stage reflection topology [22] using a circulator or coupler with appropriate reflective terminations. Large range phase shifters at microwave frequencies have been designed recently as a cascade of smaller range single stage shifters [23][24]. Another method of obtaining large range linear phase shift at microwave frequency is by detuning the tank circuit of an injection locked oscillator (ILO) [25]. Both of these phase shifter methods tend to result in complicated microwave

circuitry.

A novel and effective method of realizing full 360 degree linear phase control was proposed as a result of this research work [26][27]. This method employs a microwave frequency multiplier on the output of a highly linear fractional range phase shifter. If the baseband binary signal is integrated prior to phase modulation, the resulting modulated signal is CPFSK. The functional block diagram for this method is shown in Figure 3.1. The fractional phase shifter has a phase shift range of $2\pi/N$ radians, where N is an integer. The factor N is chosen to relax the phase linearity requirement of the fractional phase shifter to a portion of the full 2π range. This makes the fractional phase shifter realizable in hardware [28]. A stable subharmonic reference signal, at $1/N$ times the output frequency, is injected into the fractional phase shifter and the phase of the reference signal is modulated continuously over a $\pm\pi/N$ radian range. This provides a CPFSK modulated output signal at $1/N$ times the output frequency with a modulation index of $0.5/N$. The fractional CPFSK signal is fed to a $\times N$ frequency/phase multiplier which translates the modulated subharmonic reference signal to the desired output frequency and restores the modulation index to that of MSK (0.5).

The architecture shown in Figure 3.1 represents a simple direct low power microwave MSK, and general CPM, modulator. If higher transmitter output levels are required, an efficient Class C [19] power amplifier can be used on the output. Alternatively, a power oscillator, operating at the transmit frequency, can be phase locked to the MSK modulated signal [29]. Another possibility is using the MSK modulated signal to injection lock a power oscillator or antenna array.

With baseband Gaussian prefiltering, the architecture shown in Figure 3.1 can also be used to generate frequency stable GMSK modulation at microwave or millimeter-wave frequency. Microwave hardware has been de-

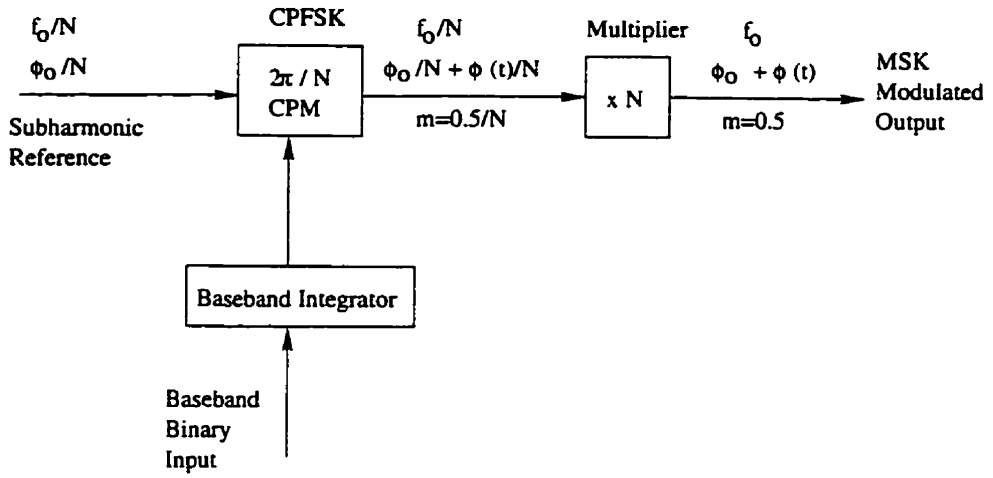


Figure 3.1 MSK modulation using fractional CPFSK and a frequency/phase multiplier.

signed for this architecture at 18 GHz to verify the feasibility of GMSK generation in this manner. Chapters 4 to 6 describe this modulator realization in detail.

There are several ways to apply Gaussian spectral shaping to the MSK modulated signal. The two most practical methods are baseband prefiltering, and controlling the PLL loop response, if a PLL is being used on the output of the CPM modulator. In the next section, application of the Gaussian filtering is described.

3.2 Gaussian Spectral Shaping

As discussed, MSK is not generally suitable in the radio environment, as the sidelobes of the MSK modulated signal roll off slowly and spill over into adjacent radio channels. To achieve the spectral efficiency required in the mobile environment, the MSK modulated signal spectrum must be filtered, to remove most of the side-lobe power and limit the transmitted signal to the main lobe of the MSK modulated signal.

3.2.1 Baseband Prefiltering

The Gaussian filtering can be applied to the binary information signal before modulation, for the modulator shown in Figure 3.1. On first glance, one might suspect that the required Gaussian filter response will be altered as a result of nonlinear multiplication. Fortunately, this is not the case, as the nonlinearity produces linear phase multiplication. As the control voltage is proportional to the fractional phase modulator phase shift, the Gaussian filtering can be applied directly to the control voltage. The filtered, fractionally modulated carrier phase will be correctly scaled by the linear phase multiplication to produce the desired Gaussian filtering effect. Therefore, the modulating voltage waveforms must be scaled for peak to peak voltage levels representing a peak to peak phase shift range of $2\pi/N$ radians in the fractional phase shifter. The complete 2π phase shift range is restored by the frequency/phase multiplier.

The binary information signal must be integrated prior to modulation, as discussed above. However, practical integration range cannot go unbounded and the control voltage must be restricted to within the $\pm\pi$ radian range of the phase shifter. Therefore, a voltage discontinuity is required at the $\pm\pi$ radian boundary, to account for the phase wrapping of 2π radians. Ideally, the voltage discontinuity should occur instantaneously to maintain continuous phase at the $\pm\pi$ radian boundary. Also, the voltage discontinuity must remain unfiltered by the Gaussian filter. Managing this voltage discontinuity is one of the major concerns with this modulation method, as a non-instantaneous transition causes an unwanted output phase trajectory at the $\pm\pi$ radian boundary. This effect is demonstrated in Chapter 6. Waveforms representing the desired modulating voltage waveform including discontinuity are shown in Figure 3.2 for various values of BT_b.

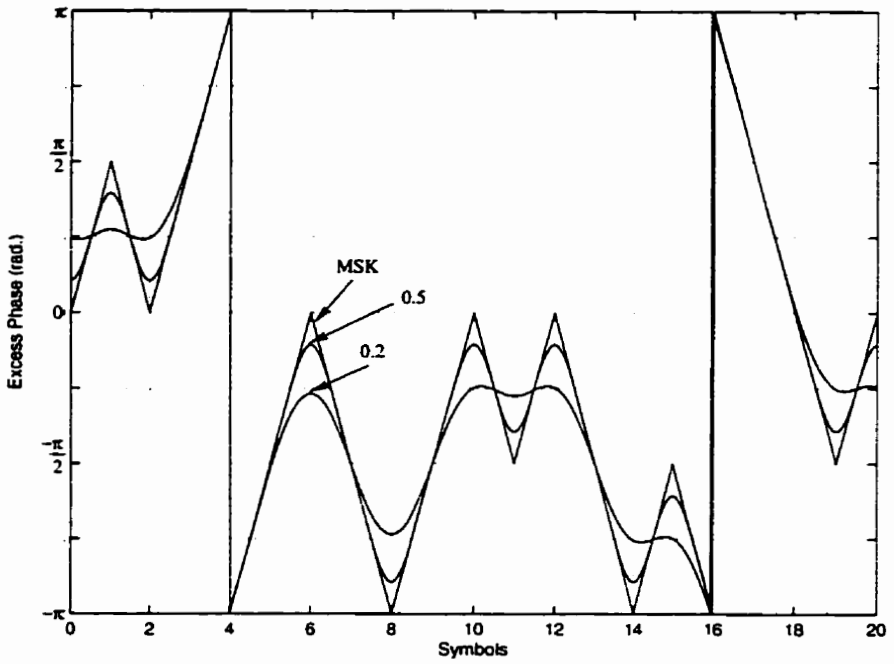


Figure 3.2 Baseband prefiltered modulation signal with voltage discontinuity for various values of BT_b.

3.2.2 PLL Response Shaping

If a high power PLO is used on the output of the MSK modulator, the PLL loop response can be designed to provide Gaussian filtering of the carrier phase [29][30]. This provides an alternative to baseband prefiltering which may result in simpler baseband hardware. One advantage in using the PLL to perform Gaussian filtering is a PLL loop filter which is simpler than an equivalent baseband Gaussian lowpass filter. Also, the modulator is inherently less susceptible to phase discontinuity at the $\pm\pi$ boundary, since the loop response is slow with respect to the discontinuity. This method is also appropriate for use with an MSK modulated signal generated by other methods than the proposed CPM modulator. The method is described below.

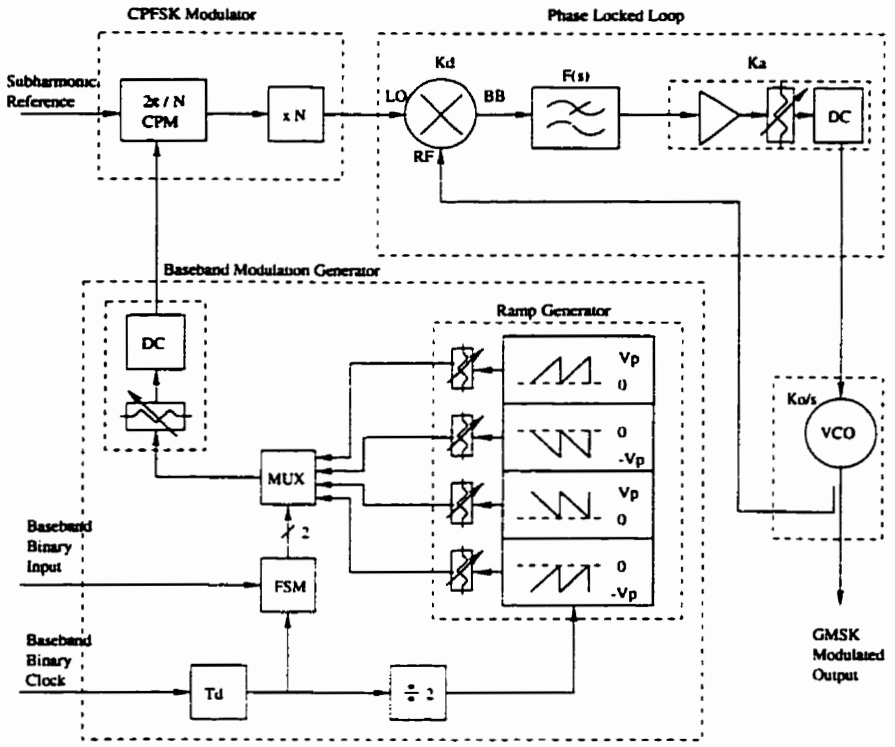


Figure 3.3 Functional block diagram of direct GMSK modulator.

3.3 Direct GMSK Modulator with PLL

The functional block diagram of the direct GMSK modulator with PLL is shown in Figure 3.3. An MSK modulated carrier signal is generated as a reference signal for the PLL at the desired output microwave transmit frequency using the full range CPM architecture described above. The PLL architecture is also suitable for use with an MSK input signal generated by any means.

The baseband modulation generator provides the integration function to the baseband signal by selecting various sawtooth waveforms representing all possible phase transitions in the output excess phase trellis. The ramp generator slope is set to provide a modulation index of $0.5/N$ at the output of the fractional phase shifter. Memory is employed to account for phase wrapping at the $\pm\pi/N$ boundaries. The modulation generator shown in Figure 3.3 is

an analog circuit realization [30]. An alternative analog modulation generator could be realized as an op-amp integrator circuit with phase wrapping control. The baseband integration function can also be realized using digital circuitry. This was the method used to test the prototype modulator circuit presented in Chapter 6.

The MSK modulated signal is fed to a PLL centred at the desired output microwave transmit frequency. The PLL allows the VCO to frequency track the stable MSK modulated input signal, while providing Gaussian filtering to convert the input MSK signal spectrum to the GMSK signal spectrum at the VCO output. The mixer/phase detector produces a voltage error signal which is the recovered baseband information signal with Gaussian filtering. The error signal directly controls the frequency of the output high power VCO to maintain phase lock to the input signal, and realize frequency tracking. As a result of the feedback in the PLL, the loop lowpass filter response is not the same as the desired Gaussian filter response, but is modified since the PLL provides a pole to the overall loop response. The PLL response characteristics and the loop lowpass filter response are described in detail in the following sections.

3.3.1 Phase Locked Loop Response

Assuming that the PLL is phase locked and that the mixer/phase detector is operating in the "linear" region of its sinusoidal phase detection characteristic, the loop equivalent lowpass frequency response is

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{KF(s)}{s + KF(s)}, \tag{3.1}$$

where $K = K_d K_o$ is the loop gain, K_d is the phase detector proportionality constant in volts/radian, K_o is the VCO sensitivity in radians/second-volt, $F(s)$ is the baseband loop filter response, $\theta_i(s)$ is the phase of the input

signal, and $\theta_o(s)$ is the phase of the output signal.

To realize Gaussian filtering, the loop response of Equation 3.1 must approximate the Gaussian lowpass filter response. The ideal Gaussian lowpass filter response [18], $H(s)$, has constant group delay and exponentially decaying amplitude response given by Equation 2.9. Setting Equation 3.1 equal to $H(s)$ gives the ideal loop filter response for Gaussian filtering as

$$F(s) = \frac{s}{K} \frac{H(s)}{1 - H(s)}. \tag{3.2}$$

Equation 3.2 demonstrates that the loop filter response is modified from the desired Gaussian response to account for the effect of the PLL. The next section describes a method of approximating the filter response of Equation 3.2.

3.3.2 Modified Gaussian Filter Response

The Gaussian filter response, $H(s)$, is approximated by applying a Taylor series expansion to $|H(j\omega T_b)|^2$ in Equation 2.9. Simplification and substitution into Equation 3.2 gives the modified Gaussian filter response

$$F(sT_b) = \frac{\sqrt{n!}(\sqrt{2}k)^{-n}(KT_b)^{-1}}{(sT_b)^{n-1} + \cdots + c_2 k^{3-n}(sT_b)^2 + c_1 k^{2-n}(sT_b) + c_0 k^{1-n}}, \tag{3.3}$$

where n is the order of the Taylor series and

$$k = \frac{\sqrt{\ln 2}}{2\pi\sqrt{2}BT_b}. \tag{3.4}$$

The denominator polynomial of Equation 3.3 is shown in Table 3.1 for Gaussian filters up to the $8th$ order ($7th$ order modified Gaussian filter).

The baseband loop filter amplitude response, $|F'(ksT_b)|$, is shown in Figure 3.4 for $BT_b = 0.5$ and various orders. The filter, $F'(ksT_b)$, implements the

Table 3.1 Modified Gaussian Filter Polynomial Coefficients

Order	c_7	c_6	c_5	c_4	c_3	c_2	c_1	c_0
2							1.000	1.553
3						1.000	2.517	2.419
4					1.000	3.585	5.428	4.032
5				1.000	4.748	10.021	11.572	7.223
6			1.000	5.996	16.480	26.234	25.257	13.831
7		1.000	7.326	25.087	51.506	67.890	57.051	28.138
8	1.000	8.732	36.122	91.654	154.87	177.37	133.76	60.472

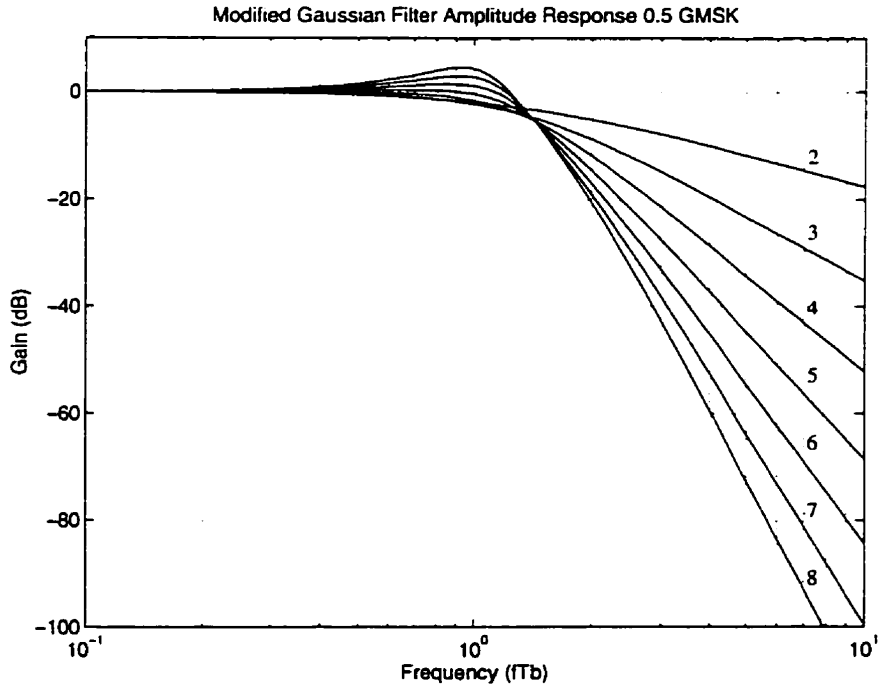


Figure 3.4 PLL baseband loop filter amplitude response for various Gaussian filter orders ($BT_b = 0.5$).

denominator portion of the modified Gaussian filter response of Equation 3.3 as

$$F'(ksT_b) = \frac{c_0}{(ksT_b)^{n-1} + \cdots + c_2(ksT_b)^2 + c_1(ksT_b) + c_0}. \tag{3.5}$$

The variable gain block, K_a, is used to adjust the PLL open loop gain to match that required by the modified Gaussian filter response of Equation 3.3 and provide the desired closed loop Gaussian filter response. The nominal value of K_a is

$$K_a = \frac{\sqrt{n!/2^n}}{KT_b c_o k} = \left(\frac{\pi^2 n!}{2^{n-3}\ln 2}\right)^{\frac{1}{2}} \frac{BT_b}{KT_b c_o}. \tag{3.6}$$

The baseband loop filter response of Figure 3.4 shows that filters of $5th$ or higher order require gain for realization. Therefore, filters of $4th$ order or lower result in the simplest baseband circuit solution and can be realized as passive ladder circuits.

This analysis demonstrates that the order of the baseband loop filter is reduced by one from the desired Gaussian filter response as one pole is contributed by the PLL.

In the next section, GMSK modulation performance in the presence of loop imperfections is discussed.

3.3.3 Phase Locked Loop Imperfections

The performance of this direct GMSK modulation method is degraded by imperfections in the PLL components. The PLL response of Equation 3.1 is based on the assumption that the phase detector is linear. Most phase detectors at microwave frequency are mixers, which have a sinusoidal rather than linear phase detection characteristic and this nonlinearity affects the loop response. Also, practical PLL components have delay, which also affects

the loop response.

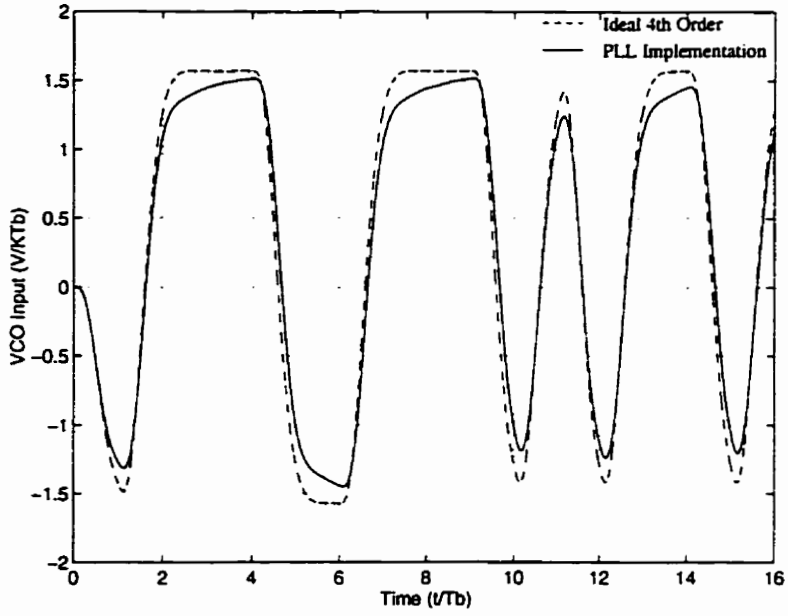
Baseband time simulations were performed using Matlab Simulink© software to ascertain the effect of these PLL imperfections on the transient performance in obtaining GMSK. The simulation included a sinusoidal phase detector and provision for adding excess baseband loop delay. The effects of loop imperfections are discussed in the following sections.

Sinusoidal Phase Detector

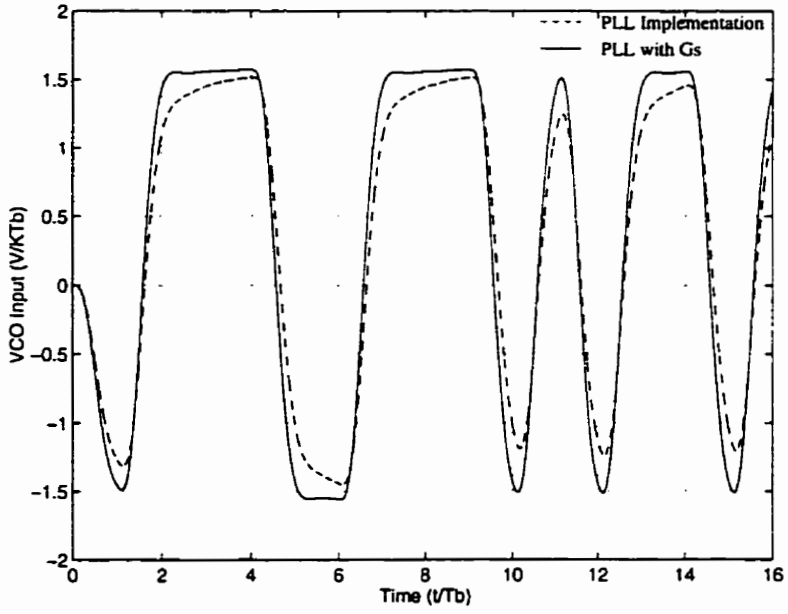
Initially, the excess delay is set to zero to observe the effect of the sinusoidal phase detector characteristic on the loop response. Figure 3.5(a) shows the closed loop signal at the VCO voltage control port for $BT_b = 0.5$ and a $4th$ order Gaussian filter approximation. Figure 3.5(a) also shows the ideal $4th$ order Gaussian filter response for comparison. It is apparent from Figure 3.5(a) that the closed loop response has been altered by the sinusoidal phase detector characteristic. This is due to the instantaneous input frequency shift ($|f_{tone}T_b| = 0.25$ for the input MSK signal) being large enough to push the phase detector error signal into the nonlinear portion of the sinusoidal characteristic. This results in open loop gain reduction. The open loop gain reduction decreases the output frequency deviation and distorts the closed loop response from the desired Gaussian response.

The sinusoidal phase detector distortion manifests itself as ISI in the modulated output signal. This behaviour is demonstrated in Figure 3.6, which shows the in-phase eye diagram for the coherently demodulated PLL output compared to an ideal $4th$ order Gaussian filter approximation, with $BT_b = 0.5$. The severity of the sinusoidal phase detector distortion depends on the order of the Gaussian filter approximation, and is more severe as the order increases.

The increased closed loop distortion with increasing Gaussian filter order

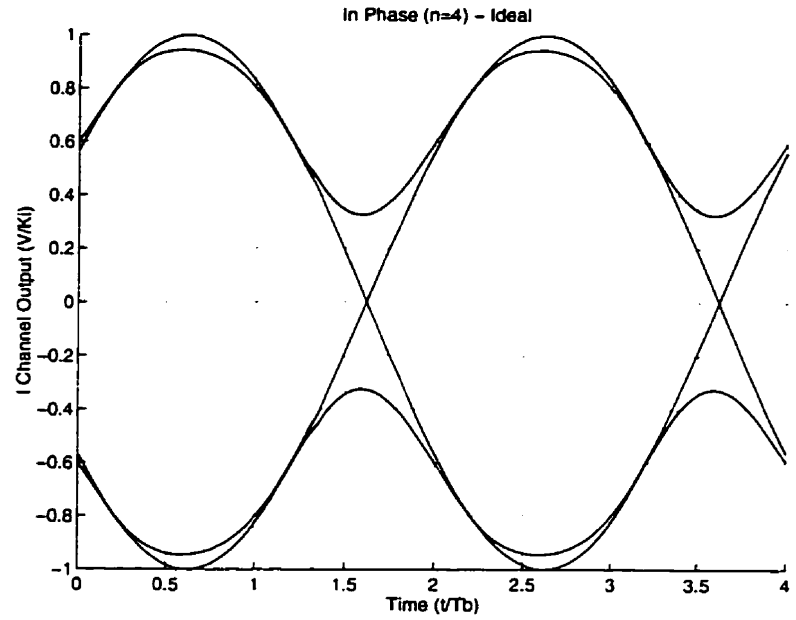


(a)

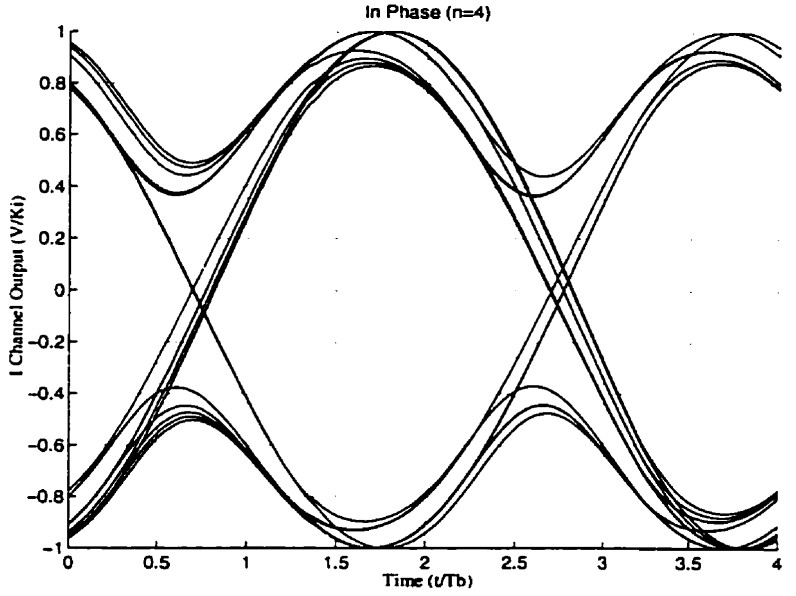


(b)

Figure 3.5 VCO closed loop input signal for $4th$ order Gaussian filter ($BT_b = 0.5$): (a) Ideal $4th$ order filter and effect of sinusoidal phase detector; (b) Sinusoidal phase detector and open loop gain correction, $G_s = 1.2$.



(a)



(b)

Figure 3.6 Eye diagrams for coherently demodulated output ($BT_b = 0.5$): (a) Ideal $4th$ order Gaussian filter; (b) $4th$ order Gaussian PLL implementation with sinusoidal phase detector.

can be explained by considering the loop tracking bandwidth. The frequency offset is $f_{tone}T_b = \pm 0.25$ for the input MSK signal. The maximum tracking bandwidth with a sinusoidal phase detector is [31]

$$|\Delta\omega_i| = KF(0), \tag{3.7}$$

where $|\Delta\omega_i|$ is the input signal frequency offset and $F(0)$ is the DC gain of the loop filter. Generally, an increase in the loop tracking bandwidth is obtained by increasing the loop gain, K, or the loop filter DC gain, $F(0)$. In this application, the loop filter DC gain, $F(0)$, is fixed at K_a which is a function of K, as shown in Equation 3.6. Therefore, increasing K requires a corresponding decrease in K_a in order to maintain the closed loop Gaussian response. Therefore, the tracking bandwidth of Equation 3.7 is fixed, for a given Gaussian filter order and BT_b value, at

$$|\Delta f_i T_b| = \left(\frac{\pi^2 n!}{2^{n-3}\ln 2}\right)^{\frac{1}{2}} \frac{BT_b}{2\pi c_o}. \tag{3.8}$$

The tracking range for a $4th$ order Gaussian filter approximation with $BT_b = 0.5$ is calculated to be $|\Delta f_i T_b| = 0.26$ from Equation 3.8, which indicates that the input MSK frequency offset of $|\Delta f_{tone}T_b| = 0.25$ is at the limit of the loop tracking range. The tracking range for a $2nd$ order Gaussian filter approximation is $|\Delta f_i T_b| = 0.39$, which is greater than the $4th$ order approximation due to an increase in open loop gain. This accounts for the increase in loop distortion as a function of Gaussian filter approximation order. The loop tracking range also decreases as BT_b decreases. Methods of compensating for the sinusoidal phase detector characteristic are discussed below.

Increasing the Loop Gain

The decrease in open loop gain from the sinusoidal phase detector can be compensated to some extent by an increase in the loop gain constant, K_a. This involves modification of Equation 3.6 to include a sinusoidal detector gain correction factor, G_s, as

$$K_a = \left(\frac{\pi^2 n!}{2^{n-3}\ln 2}\right)^{\frac{1}{2}} \frac{BT_b G_s}{KT_b c_o}. \tag{3.9}$$

Inclusion of the gain correction factor, G_s, results in significant improvement in the closed loop VCO input signal distortion, as shown in Figure 3.5(b) with $G_s = 1.2$. The eye diagram for the coherently demodulated PLL output is comparable to that of Figure 3.6 for the ideal case. The gain correction factor also increases the loop tracking bandwidth by a factor of G_s, giving the phase detector some range to track VCO frequency drift.

Microwave Frequency Divider

The gain correction factor, G_s, can only provide adequate compensation for combinations of Gaussian filter approximation order and BT_b value which result in a loop tracking range that is comparable to the input signal peak frequency deviation, such as a $4th$ order Gaussian filter approximation with $BT_b = 0.5$. High order and/or low BT_b value filter approximations cannot, generally, be realized using simple open loop gain correction to increase loop bandwidth as the loop bandwidth is substantially less than the input signal peak frequency deviation.

In these situations, a microwave frequency divider, with an integer frequency division factor of M, in the feedback path of the PLL can be used to reduce the peak phase detector error from the highly nonlinear portion of the sinusoidal phase detector characteristic. The PLL input signal in this case is a CPFSK modulated signal at $1/M$ times the PLL output frequency with a

Table 3.2 Realistic PLL GMSK Implementation Parameters

BT_b	Order	Divider (M)	Bandwidth ($\lvert\Delta f_i T_b\rvert$)
0.3	2	2	0.464
	3	2	0.365
	4	2	0.310
0.5	2	1	0.387
	3	1	0.304
	4	1	0.258
0.7	2	1	0.541
	3	1	0.426
	4	1	0.361

modulation index of $0.5/M$. The loop gain constant, K_a, from Equation 3.9 must be multiplied by M, to maintain the desired closed loop Gaussian filter response, as

$$K_{aM} = \left(\frac{\pi^2 n!}{2^{n-3}\ln 2}\right)^{\frac{1}{2}} \frac{BT_b G_s M}{K T_b c_o}. \tag{3.10}$$

This also results in an increase in the tracking bandwidth of Equation 3.8 by a factor of M. Table 3.2 provides guidelines for the selection of Gaussian filter approximation order and feedback frequency divider ratio for realizable loop implementations.

Loop Delay

Excess time delay in the PLL components also causes distortion in the closed loop response. Provided that the input frequency deviation is within the loop bandwidth and the delay is less than that tolerated by the open loop phase margin, an additional gain correction factor, G_d, can be added

to the loop gain constant, K_{aM}, from Equation 3.10 to partially compensate for the effects of excess loop delay as

$$K_{aM} = \left(\frac{\pi^2 n!}{2^{n-3}\ln 2}\right)^{\frac{1}{2}} \frac{BT_b G_s G_d M}{K T_b c_o}. \tag{3.11}$$

VCO Output Frequency Stability

The VCO free-running output frequency stability also imposes practical performance limitations. As the VCO output frequency drifts from the loop centre frequency, the phase detector error signal DC level shifts from zero, into the nonlinear portion of the sinusoidal characteristic. In this situation, the loop gain compensation value for the sinusoidal detector characteristic, G_s, is no longer optimal, resulting in a distorted VCO input signal and the return of ISI in the modulated output signal. The VCO frequency stability must be selected to maintain the desired level of ISI in the modulated output signal. The required VCO output frequency stability is defined as

$$\Delta f_n = \left|\frac{f_{drift}}{f_o}\right| = \left|\frac{f_{drift_n} f_b}{f_o}\right|, \tag{3.12}$$

where $f_{drift_n} = f_{drift} T_b$ is the tolerable VCO drift normalized to the bit rate, T_b. Alternatively, the minimum bit rate, f_b, is defined for a given VCO stability as

$$f_b = \frac{|\Delta f_n| f_o}{f_{drift_n}}. \tag{3.13}$$

Figure 3.7, shows the effect of a VCO frequency drift of $0.01/T_b$ on the eye diagrams for the coherently demodulated PLL output excess phase of a $4th$ order Gaussian filter approximation, with $BT_b = 0.5$, and an excess loop delay of $0.1T_b$. This combination is shown for illustrative purposes as it represents one of the worst cases expected. This is because the loop

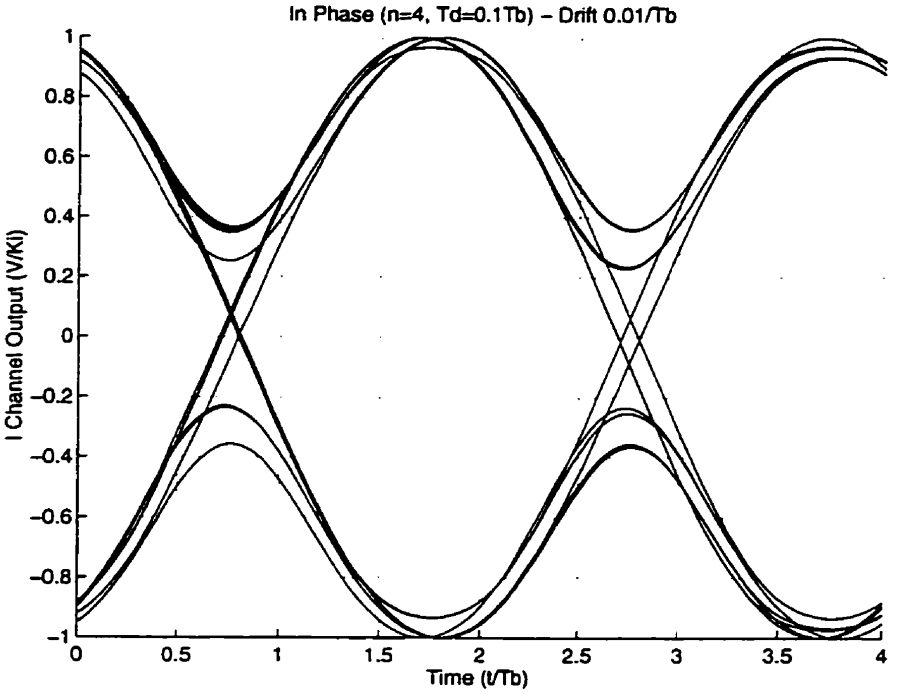


Figure 3.7 Eye diagram for coherently demodulated output of $4th$ order Gaussian PLL implementation with sinusoidal phase detector, excess loop delay of $0.1T_b$, and VCO frequency drift of $0.01/T_b$ ($BT_b = 0.5$).

bandwidth is only marginally above the input frequency deviation, and the required gain compensation factor, G_s is high. For example, the $2nd$ order Gaussian filter approximation, with $BT_b = 0.5$, can tolerate almost three times as much VCO drift for comparable ISI.

3.4 Summary

An elegant hardware architecture for direct GMSK modulation at microwave and millimeter-wave frequencies is realized using indirect FM and a full range CPM modulator, with the Gaussian filter response imposed on the integrated baseband modulating signal. An effective and novel modulator solution is obtained using a fractional phase shifter and a frequency/phase

multiplier. This architecture is suitable for low level GMSK modulation. If higher output levels are required, an efficient power amplifier or phase locked power oscillator can be used on the output of the modulator.

The use of a phase locked power oscillator on the modulator output also provides the possibility of designing the PLL response to provide the Gaussian filtering, an an option to prefiltering. PLL imperfections such as nonlinear phase detector distortion and excess loop delay degrade the loop response from the desired Gaussian response, resulting in ISI in the modulated output signal. Control of the loop gain and/or inclusion of a frequency divider in the PLL feedback path reduces this loop distortion significantly. As a result of the nonlinear phase detector, loop tracking bandwidth is limited, and a trade-off between VCO free-running output frequency stability and modulated output signal distortion exists. Appropriate choice of Gaussian filter approximation order and control of important loop parameters such as loop delay, loop gain, and VCO frequency stability results in acceptable performance.

The direct GMSK architecture based on a fractional phase shifter and a frequency/phase multiplier results in a simple, cost effective hardware solution requiring very few components which makes it an attractive option to consider in the development of future high capacity digital radio systems. In the next chapters, realization of this modulator at 18 GHz is discussed in detail.

4. DIRECT GMSK MODULATOR DESIGN

A direct microwave GMSK modulator hardware architecture based on a fractional CPM modulator and frequency/phase multiplier was proposed in the previous chapters. In order to evaluate the feasibility of this method, realistic microwave hardware was designed. This chapter presents the important microwave hardware design considerations for realization of the direct microwave GMSK modulator at a transmit frequency of 18 GHz.

4.1 Linear Phase Shifter

Linear phase shifters find use in a number of applications requiring continuous linear phase control of a microwave carrier signal. Examples of such applications include continuous phase modulators, phase synchronization of antenna and oscillator arrays, and phased array antenna beam steering.

Many microwave linear phase shifters are based on a single stage reflection topology [22][32] using a circulator or coupler with appropriate reflective terminations. This topology is shown in Figure 4.1 for a circulator. This is the basic topology used for microwave phase shifters, delay lines, and variable attenuators, with the only major difference being the reflective terminations [22]. For phase shifters the terminations are, generally, reactive to avoid unnecessary loss through the phase shifter, and are often comprised of a grounded series combination of an inductor and a capacitor [21]. If the capacitor is variable, the reactance of the termination, and thus the phase of the voltage reflection coefficient, can be controlled to provide variable phase shift in the reflected signal. Reverse biased varactor diodes or interdigitated planar Schottky varactor diodes (IPSVD) [32], which are created by connecting

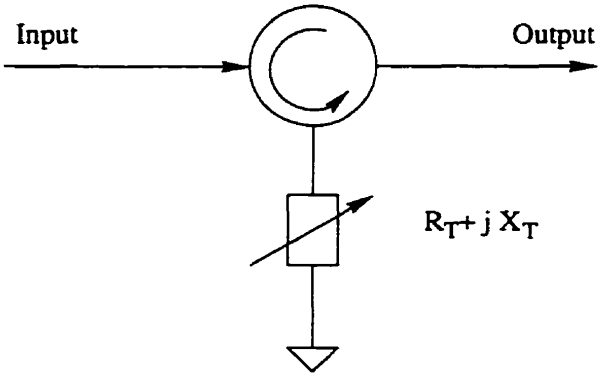


Figure 4.1 Single stage microwave reflective circuit topology.

the drain and source of a field effect transistor (FET) together, are generally used to provide variable capacitance control. In MMIC design, IPSVDs are more commonly used due to difficulties in realizing varactor diodes [32].

It is very difficult to design the reflective terminations to provide linear phase shift over a very large range, using a single stage reflective phase shifter. The linearity problem is further complicated for MIC implementations at microwave frequencies above 3 GHz, where the required minimum varactor capacitance value becomes comparable to the varactor parasitic package capacitance [28]. The package capacitance at these frequencies has a dramatic effect on the phase shift linearity and must be considered in the implementation. An abrupt junction varactor diode with $\gamma = 0.5$, where γ is the junction doping profile, is not necessarily the best choice for phase shift linearity, and hyperabrupt junction varactors may produce better results [28].

4.1.1 Reflection Phase Shifter

A coupler is more suitable for planer microstrip circuit implementation than a circulator and was chosen for the reflection phase shifter. The coupler must provide equal power division and a phase shift of $\pi/2$ radians at the through and coupled output ports. This is necessary to maintain a match at the input port and reflect all input power to the isolated port. A coupler that

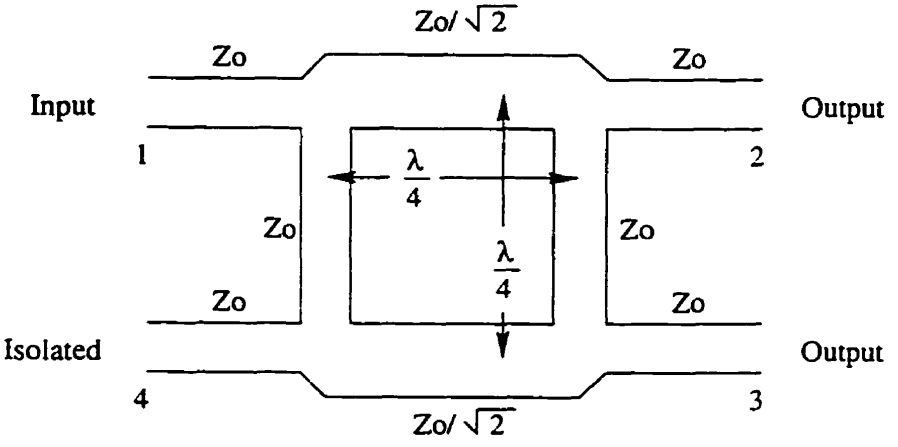


Figure 4.2 Quadrature hybrid coupler.

is suitable for this purpose is the quadrature hybrid coupler [33]. A Lange coupler [33] is more complicated than a quadrature hybrid coupler, but could also be used if wider bandwidth is required [32].

The quadrature hybrid coupler is shown in Figure 4.2. The length of the hybrid branches is $\lambda/4$, the characteristic impedance of the through branches is $Z_o/\sqrt{2}$, and the characteristic impedance of the coupled branches is Z_o, where Z_o is the characteristic impedance of the system. The four port scattering parameter matrix, $[S]$, for the coupler, assuming that all four ports are matched, is given by [33]

$$[S] = \frac{-1}{\sqrt{2}} \begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix}. \tag{4.1}$$

Assuming that the coupled ports (ports 2 and 3) are terminated in the characteristic impedance of the line, Z_o, then there is equal power division and $\pi/2$ radian phase shift between ports 2 and 3, perfect match at port 1, and perfect isolation between ports 1 and 4, for the ideal coupler. If ports 2 and 3 are terminated in purely reactive loads (including open or short

circuits) then all input power is reflected from the terminations, re-enters the coupler, and adds vectorally at ports 1 and 4. The desired characteristic of the reflection phase shifter is that this reflected power combine constructively at the isolated port and destructively at the input port. In an ideal coupler, these two conditions represent a perfect match at the input (port 1) and no loss from input to output (port 4). For an incident wave at port 1, with voltage $V_1^+ = 1$, the voltages of the reflected waves emerging at ports 1 and 4 can be written as

$$V_{1/2}^- = (-\frac{j}{\sqrt{2}})(\Gamma_2)(-\frac{j}{\sqrt{2}}) = -\frac{1}{2}\Gamma_2, \tag{4.2}$$

$$V_{1/3}^- = (-\frac{1}{\sqrt{2}})(\Gamma_3)(-\frac{1}{\sqrt{2}}) = \frac{1}{2}\Gamma_3, \tag{4.3}$$

$$V_{4/2}^- = (-\frac{j}{\sqrt{2}})(\Gamma_2)(-\frac{1}{\sqrt{2}}) = \frac{j}{2}\Gamma_2, \tag{4.4}$$

$$V_{4/3}^- = (-\frac{1}{\sqrt{2}})(\Gamma_3)(-\frac{j}{\sqrt{2}}) = \frac{j}{2}\Gamma_3, \tag{4.5}$$

where $V_{1/2}^-$ and $V_{1/3}^-$ represent the voltages of the reflected signal out of port 1, as reflected from ports 2 and 3, $V_{4/2}^-$ and $V_{4/3}^-$ represent the voltages of the reflected signal out of port 4, as reflected from ports 2 and 3, and Γ_2 and Γ_3 are the complex voltage reflection coefficients at the terminated ports. The total signal out of ports 1 and 4 can be obtained using superposition, by adding Equations 4.2 and 4.3 and Equations 4.4 and 4.5, vectorally. This addition yields

$$V_1^- = \frac{1}{2}(\Gamma_3 - \Gamma_2), \tag{4.6}$$

$$V_4^- = \frac{J}{2}(\Gamma_3 + \Gamma_2). \tag{4.7}$$

From Equations 4.6 and 4.7, it is apparent that if the reflection coefficients for the terminations at ports 2 and 3 are equal and purely reactive, then

$$\Gamma_3 = \Gamma_2 = \Gamma = e^{J\phi}, \tag{4.8}$$

where ϕ is the angle of the voltage reflection coefficient, and

$$V_1^- = 0, \tag{4.9}$$

$$V_4^- = e^{J(\frac{\pi}{2}+\phi)}. \tag{4.10}$$

Equations 4.9 and 4.10 verify the ideal assumptions for the reflection phase shifter of perfect match at the input, as no voltage is reflected from port 1, and no loss from port 1 to 4, as $|V_4^-| = |V_1^+| = 1$. A good input match and low loss is only maintained, however, if the terminations are well matched. It is also apparent from Equation 4.10 that the phase shift through the coupler can be controlled by varying the phase of the reflection coefficient at the terminations. Also, the phase shift through the coupler is the same as the phase of the voltage reflection coefficient, offset by $\pi/2$ radians. This is the principle of the reflection phase shifter.

4.1.2 Reactive Terminations

In Equation 4.10, it was shown that the phase shift through a reflection phase shifter can be controlled by varying the phase of the reflection coefficient of the reactive terminations. It is apparent, however, that linear control of the reflection coefficient phase is not possible by linearly varying the reactance of the termination. This fact is evident by observing the nonlinear

spacing of constant reactance lines as the lines intersect the $R = 0$ circle on a Smith Chart [33]. Thus, the problem in designing the reflective terminations becomes one of choosing a nonlinear variable reactance device that provides reflective phase shift that is proportional to linear variation in the reactance control signal. One suitable device that provides nonlinear capacitance (and thus reactance) control by means of voltage control is a reverse biased varactor diode. Varactor diodes with sufficiently high quality factor (Q) can be effectively considered purely reactive and provide very little loss in the reflected signal due to parasitic resistance.

Obtaining linear phase shift from a reflective termination can be illustrated by using a short circuit sliding termination model [21]. In this model, the reflective termination is a short circuit transmission line of length l connected to the coupler ports. In this configuration, the input signal leaves the coupler, is reflected by the short circuits, and travels a path of length $2l$ before re-entering the coupler. This results in a phase shift through the coupler of $4\pi l/\lambda$ radians in excess of the phase shift if the coupler was shorted at the ports. As the position of the short circuit is moved, the resultant change in phase shift is linear and proportional to the change in length, l.

Approximating the sliding short circuit termination behaviour with a fixed reactive termination requires that the termination reactance be matched to the reactance of a short circuit transmission line of characteristic impedance Z_o and length l [21]. The reactance of a short circuit transmission line is the tangent of the control variable (l). Therefore, the reflective termination reactance must also be the tangent function of a control variable. For varactors, the control variable must be proportional to the reverse bias voltage V. The relationship for matching to the reactance tangent function is [21]

$$\frac{X}{Z_o} = \tan(2\pi l/\lambda) = \tan(k_v V), \tag{4.11}$$

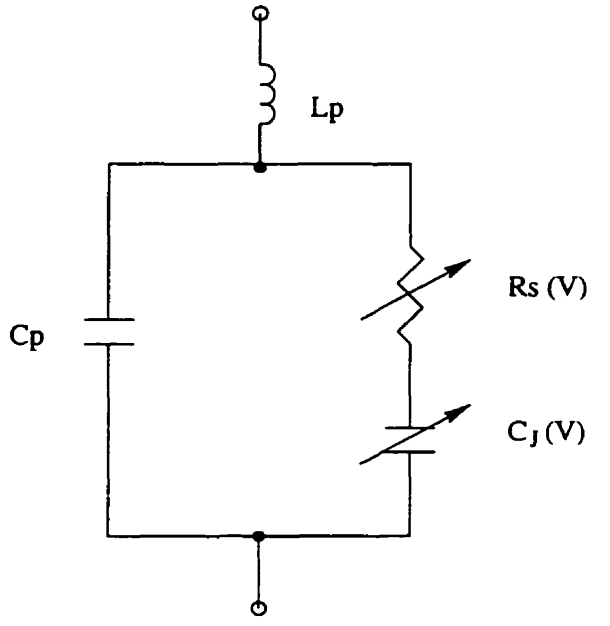


Figure 4.3 Reverse biased varactor diode model.

where $\frac{X}{Z_o}$ is the termination reactance normalized to Z_o and k_v is a constant of proportionality.

In order to match the termination reactance to the reactance tangent function, the varactor must be adequately modelled. The model for a packaged reverse biased varactor diode [34] is shown in Figure 4.3. The capacitance versus voltage (CV) relationship for the variable junction capacitance shown in Figure 4.3 is given by [35]

$$C_J = \frac{C_o}{\left(\frac{V_R}{\Phi} + 1\right)^{\gamma}}, \tag{4.12}$$

where γ is the PN junction doping profile, V_R is the applied reverse biased voltage, Φ is the diode contact potential, and C_o is the maximum diode capacitance. As long as the parasitic varactor resistance is small (ie: high Q varactor) compared to the capacitive reactance, the capacitive reactance of the varactor is essentially $C_v = C_J + C_p$, where C_J is the variable capacitance shown in Equation 4.12 and C_p is the parasitic varactor package capacitance.

An expression for the termination reactance can be written and compared to the desired reactance tangent function of Equation 4.11. A good match to the tangent function indicates a linear change in the reflection coefficient phase with respect to a linear varactor control voltage variation. Assuming a grounded series combination of an inductor and a reverse biased varactor diode, the termination reactance normalized to Z_o is

$$\frac{X_T}{Z_o} = \frac{\omega L_s}{Z_o} - \frac{1}{\omega C_v Z_o}, \tag{4.13}$$

where ω is the input angular frequency, L_s is the series inductance, and $C_v = C_J + C_p$ is the total varactor capacitance. In order to select a suitable varactor characteristic to match to the reactance tangent function, shown in Equation 4.11, it is useful to normalize the reverse biased voltage, so different varactors can be easily compared. This is done as follows

$$V_N = \frac{V_R - \Phi}{V_{max} - \Phi}, \tag{4.14}$$

where $0 \leq V_N \leq 1$ corresponds to $-\Phi \leq V_R \leq V_{max}$, and V_{max} is the maximum reverse biased varactor voltage which corresponds to the minimum varactor capacitance. Equation 4.12 can then be written in terms of V_N as

$$C_J = \frac{C_{min}}{V_N^{\gamma}}, \tag{4.15}$$

where C_{min} is the varactor capacitance value at V_{max}. With C_J expressed as in Equation 4.15, C_{min} and L_s values can be determined for a varactor specified by γ, independent of C_o and Φ, that minimizes the error between the termination reactance curve of Equation 4.13 and the reactance tangent function curve of Equation 4.11, over a normalized reverse biased voltage range of $0 \leq V_N \leq 1$. For the minimization, the number of points used in the two functions must be equal and the reactance tangent function must be

calculated over a large enough range to give the desired phase shift. This reactance tangent function range should correspond to a termination reactance bias voltage range of $0 \leq V_N \leq 1$ for the minimization. An adequate range is $l/\lambda = 0.12$, or a phase shift of $4\pi(0.12) = 86.4$ degrees. One effective method for minimizing this error is by finding values of C_{min} and L_s that minimize the difference between the two functions on a point by point basis, in a "least squares" sense. The objective function for performing this minimization is

$$f(C_{min}, L_s) = \sum_{V_N=0}^{1} \{X[0.12(V_N - 1)] - X_T[C_{min}, L_s, V_N]\}^2, \qquad (4.16)$$

where X and X_T are given by Equations 4.11 and 4.13.

Garver [21] suggested that an abrupt junction varactor, with γ in the range of 0.5, is generally suitable for matching to the tangent function over a limited bias voltage range. As the operating frequency is increased, the required minimum varactor capacitance, C_{min}, becomes comparable to the varactor parasitic package capacitance, C_p, and a good match cannot be obtained [28]. The effect of C_p is a flattening of the CV characteristic and the termination reactance characteristic as a function of increasing bias voltage. This behaviour is demonstrated in Figure 4.4, assuming an abrupt junction varactor with maximum capacitance, $C_o = 1.5$ pF, parasitic package capacitance of $C_p = 0.15$ pF, and $\gamma = 0.47$. In Figure 4.4, the termination reactance is matched to the reactance tangent function at an operating frequency of 3.6 GHz, with $C_p = 0$, using the "least squares" criteria as in Equation 4.16, then C_p is increased to 0.15 pF. With this situation, the abrupt junction varactor, with $\gamma = 0.47$, no longer provides a good match to the tangent function, even if C_p is considered in the "least squares" minimization, as shown in Figure 4.5. The result of this mismatch to the reactance tangent function is poor phase shift linearity. Varying the varactor γ can improve the phase shift linearity.

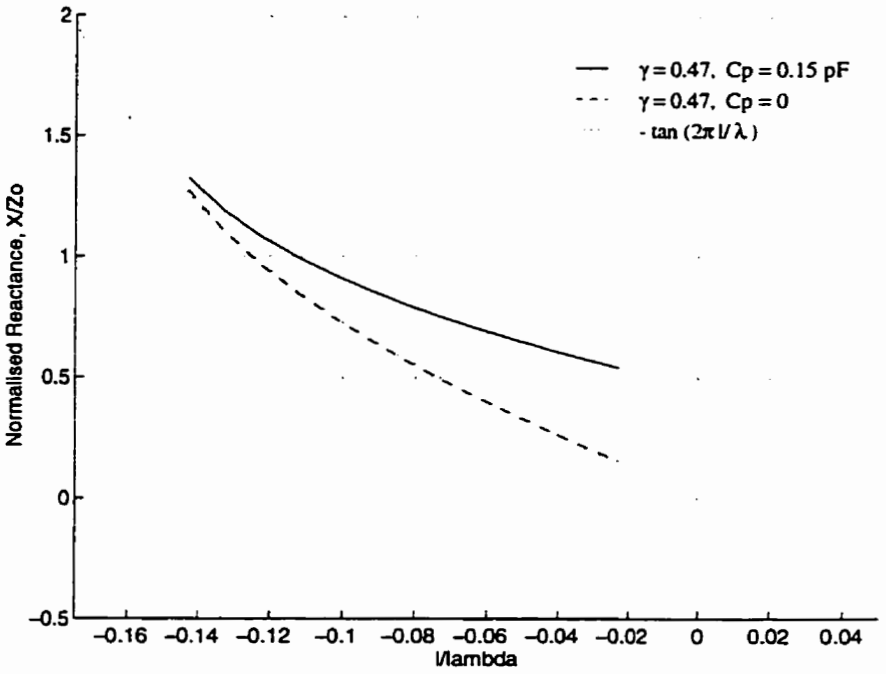


Figure 4.4 Termination reactance matched to the tangent function, $\gamma = 0.47$.

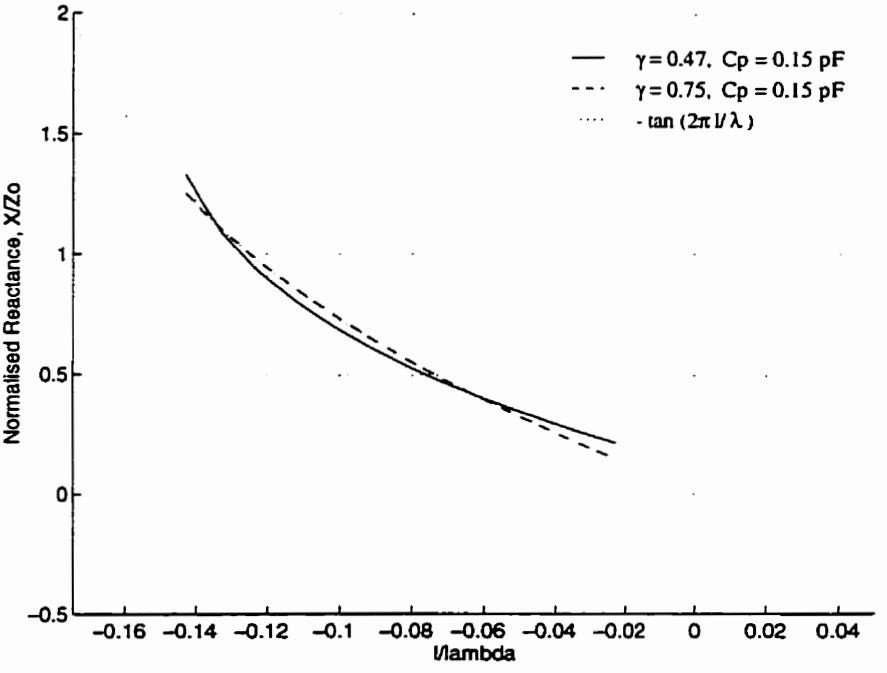


Figure 4.5 Termination reactance matched to the tangent function, $\gamma = 0.75$.

The use of a hyperabrupt junction varactor increases γ, thereby reducing the reactance characteristic flattening effect caused by parasitic package capacitance. This is because a larger capacitance change is obtained in a hyperabrupt junction varactor as compared to an abrupt junction varactor for the same change in reverse voltage. Using a hyperabrupt junction varactor, with $\gamma = 0.75$, a near optimal match to the tangent function is obtained over a limited phase shift range, with $L_s = 3.54$ nH and $C_o = 2.4$ pF, at an operating frequency of 3.6 GHz. This behaviour is shown in Figure 4.5. The minimum varactor capacitance, C_{min}, is 0.46 pF and corresponds to $V_N = 1$, or $V_R = 10.5$ V. For a hyperabrupt junction varactor with $\Phi = 1.3$ V, the reverse bias voltage range corresponding to $0 \leq V_N \leq 1$ is $-1.3 \leq V_R \leq 10.5$ V.

The effectiveness of the match to the reactance tangent function can also be demonstrated by plotting the phase of the termination reflection coefficient versus reverse bias voltage. This is determined as

$$\arg(\Gamma_T) = \arg\left(\frac{j\frac{X_T}{Z_o} - 1}{j\frac{X_T}{Z_o} + 1}\right), \tag{4.17}$$

where $\frac{X_T}{Z_o}$ is given by Equation 4.13. The termination phase shift versus reverse bias voltage is shown in Figure 4.6. From Figure 4.6, a total phase shift in excess of 80 degrees is observed. If the phase shift versus bias plot is "flattened" by adding a linear function of the form $\phi = -mV_N + b$, the phase shift linearity versus bias can be obtained. This is plotted in Figure 4.7. From Figure 4.7, the phase shift linearity is determined to be within ± 0.2 degrees from linear, over a total phase shift range of 86 degrees.

This section has demonstrated the feasibility of designing a simple, highly linear, reflection phase shifter over a fraction of the full 360 degree phase shift range, by careful consideration of the reactive terminations. The next section will explore a means to expand this linear phase shift range in excess of the

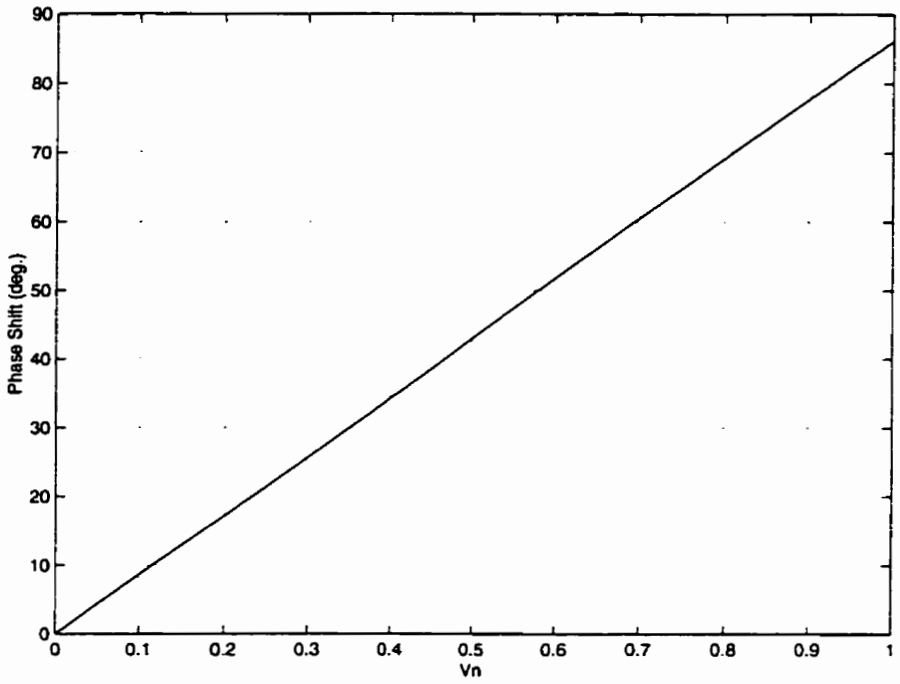


Figure 4.6 Reactive termination reflection coefficient phase shift as a function of normalized reverse biased varactor voltage.

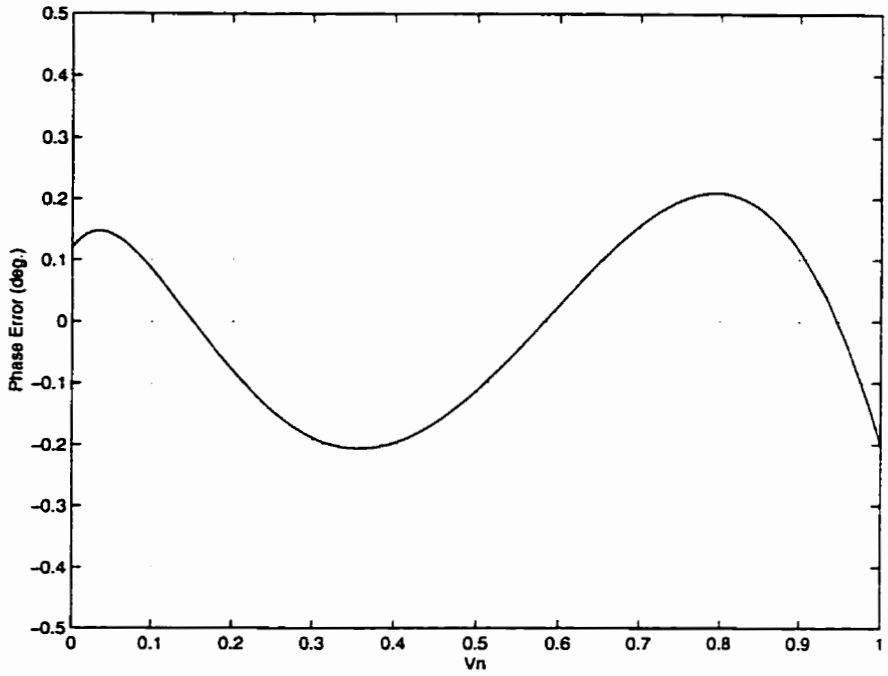


Figure 4.7 Reactive termination reflection coefficient phase shift linearity as a function of normalized reverse biased varactor voltage.

required 360 degrees.

4.2 Frequency/Phase Multiplier

Highly linear phase shift can be achieved over a typical phase shift range of less than 90 degrees [28]. Use of a frequency/phase multiplier is an attractive method of increasing this phase shift range.

Frequency multiplication principles are well known. Frequency multiplication is a process by which a nonlinear circuit is used to generate harmonics of a fundamental frequency CW input signal. The desired harmonic signal is then selected, while the fundamental frequency and all other harmonic signals are rejected, usually by a narrowband tuned circuit. This process is often used to generate stable, microwave or millimeter-wave signals.

A more subtle consequence of the nonlinear circuit response is instanta-

neous phase multiplication, by the integer harmonic number, since phase and frequency are inseparable and frequency is the time derivative of phase. This phenomenon can be demonstrated by considering the response of a nonlinear system to a single frequency CW input signal. The output voltage, $V_o(t)$, of a nonlinear system can be represented as an nth order polynomial function of the input signal, $V_i(t)$, as

$$V_o(t) = aV_i(t) + bV_i^2(t) + cV_i^3(t) + \cdots + mV_i^n(t), \tag{4.18}$$

where $a, b, ...m$ represent the magnitudes of the individual polynomial terms.

If $V_i(t) = \cos(\omega t + \phi(t))$, which is a constant envelope signal with amplitude of 1 V, angular frequency of ω radians/second, and time varying excess phase of $\phi(t)$ radians, then Equation 4.18 can be written as

$$V_o(t) = \frac{b}{2} + (a + \frac{3c}{4})\cos(\omega t + \phi(t)) + \frac{b}{2}\cos(2\omega t + 2\phi(t)) + \frac{c}{4}\cos(3\omega t + 3\phi(t)), \tag{4.19}$$

for a polynomial order in Equation 4.18 of $n = 3$. Equation 4.19 demonstrates that a nonlinear system, with an nth order component of nonlinearity, yields an output containing a signal component at $\times n$ the input signal fundamental frequency. This is the property of nonlinearity that is exploited in frequency multiplication. Also apparent from Equation 4.19 is that the instantaneous excess phase of the input signal, $\phi(t)$, is multiplied by a factor of n for an nth order nonlinearity. This is the property that is used to expand the linear phase shift range of the fractional phase shifter. The next section discusses obtaining the nonlinear circuit.

4.2.1 Nonlinearity

All real circuits exhibit some degree of nonlinearity. Usually, nonlinearity is undesirable, and attempts are made to operate under conditions that make the effects of nonlinearity negligible. However, to achieve linear frequency/phase multiplication, nonlinearity is necessary and the operation conditions must be chosen to enhance the desired nonlinear circuit effects.

Traditionally, two terminal passive devices such as varactor diodes, step-recovery diodes (SRDs), and Schottky-barrier diodes have been used as nonlinear circuit elements to design frequency multipliers at microwave frequencies [36]. Recently, three terminal active devices, such as GaAs FETs, have become popular for use as nonlinear elements in frequency multiplier design [37][38][39][40]. The use of such devices in multipliers is attractive as these multipliers usually offer greater power efficiency, bandwidth, and require fewer components then comparable diode multipliers [36]. They also provide higher isolation between input and output [37], provide gain, and are more suitable for planar microwave circuit implementation.

Diode multipliers still find applications, and have been used recently in millimeter-wave frequency multipliers [41][42] where suitable three terminal active devices are either expensive or unavailable. Varactor diode multipliers are passive and reactive, and thus, generate little additional carrier phase noise, above the inevitable multiplier phase noise degradation of $20\log(n)$ [36], where n is the multiplication factor. Active devices such as FETs contribute additional phase noise.

Despite the poorer phase noise performance, FET frequency multipliers, offer many advantages over diode multipliers and are suitable for simple, single stage planar microwave circuitry. It is for this reason that a FET multiplier architecture was chosen to provide the multiplier nonlinearity. The remainder of this chapter is dedicated to FET frequency multipliers.

4.2.2 FET Frequency Multiplier

A simple microwave frequency multiplier can be designed using a single FET nonlinear device [36] to generate harmonics of a microwave input signal. There are a variety of nonlinear mechanisms present in a FET multiplier. These include [39]:

a.) Nonlinear equivalent circuit items such as the gate to source capacitance, C_{gs}, the transconductance, g_m, and the output conductance, G_d.

b.) Biasing the FET gate such that the drain current clips when the gate voltage exceeds the forward conduction threshold (Class A current rectification).

c.) Biasing the FET gate such that the drain current clips when the gate voltage drops below the pinch-off, or turn-on, voltage, V_t (Class B current clipping).

Gopinath et. al. [37] concluded that C_{gs} contributed little to the harmonic generating effects in frequency doublers, compared to the other nonlinear effects mentioned. The nonlinearity of G_d is most prominent around the gate forward conduction region, while the variation of g_m in this region is small [39]. The nonlinearity of G_d, therefore, contributes most to the nonlinearity in the Class A current clipping mode of operation. The nonlinearity of g_m is most prominent around the gate pinch-off voltage, while G_d in this region is fairly constant [39]. The nonlinearity of g_m, therefore, enhances the nonlinearity in the Class B current clipping mode of operation.

The gate bias point and input signal level can also be selected to generate harmonics in the FET drain current. The drain current can clip if the gate voltage either exceeds the gate forward conduction threshold, or falls below the gate pinch-off voltage, or both. This clipping can be considered as a rectified sinusoidal drain current waveform, or a half sinusoidal drain current

pulse train. The drain current pulse train is a waveform that is rich in harmonics [36]. The choice of a Class A or Class B operating condition to generate the drain current pulse train depends somewhat on the application. Dow and Rosenheck [39] concluded that Class A and Class B multiplier operation was analogous to Class A and Class B power amplifier operation, in that Class A provided maximum gain while Class B provided maximum output power. Other published results, however, have been less conclusive in this respect. Rauscher [38] suggests that the Class A mode of operation involves higher DC drain current (and thus lower DC-RF power efficiency) and has a higher risk of device failure due to elevated gate current spikes, than the Class B mode of operation. For this reason, the current clipping mode of operation was chosen as a better bias alternative.

The FET gate in the current clipping mode of operation is biased at or below the turn-on voltage, V_t. If biased below V_t, the FET is actually biased at a Class C power amplifier bias point. The drain conducts only when the gate voltage exceeds the turn-on threshold. Therefore, the drain current only conducts over a fraction of the positive cycle of the input signal, and can be modelled as a train of half-cosine pulses [36]. This model is only an approximation, as a real FET will exhibit a "soft" turn-on characteristic at the gate threshold, due mainly to the decrease in transconductance near the turn-on threshold. The gate voltage and drain current waveforms for an ideal FET multiplier are shown in Figure 4.8. The peak of the drain current is labelled I_{max} and corresponds to the maximum gate voltage, $V_{g,max}$. When all harmonics, except the desired harmonic, of the drain current are short circuited, only the desired harmonic voltage can exist at the drain. This is shown in Figure 4.8, for a 2nd harmonic output resonator.

The input signal level and gate bias voltage are selected to obtain a conduction angle that maximizes the output level of the desired harmonic. An approximation relating the harmonic drain current to the FET conduction

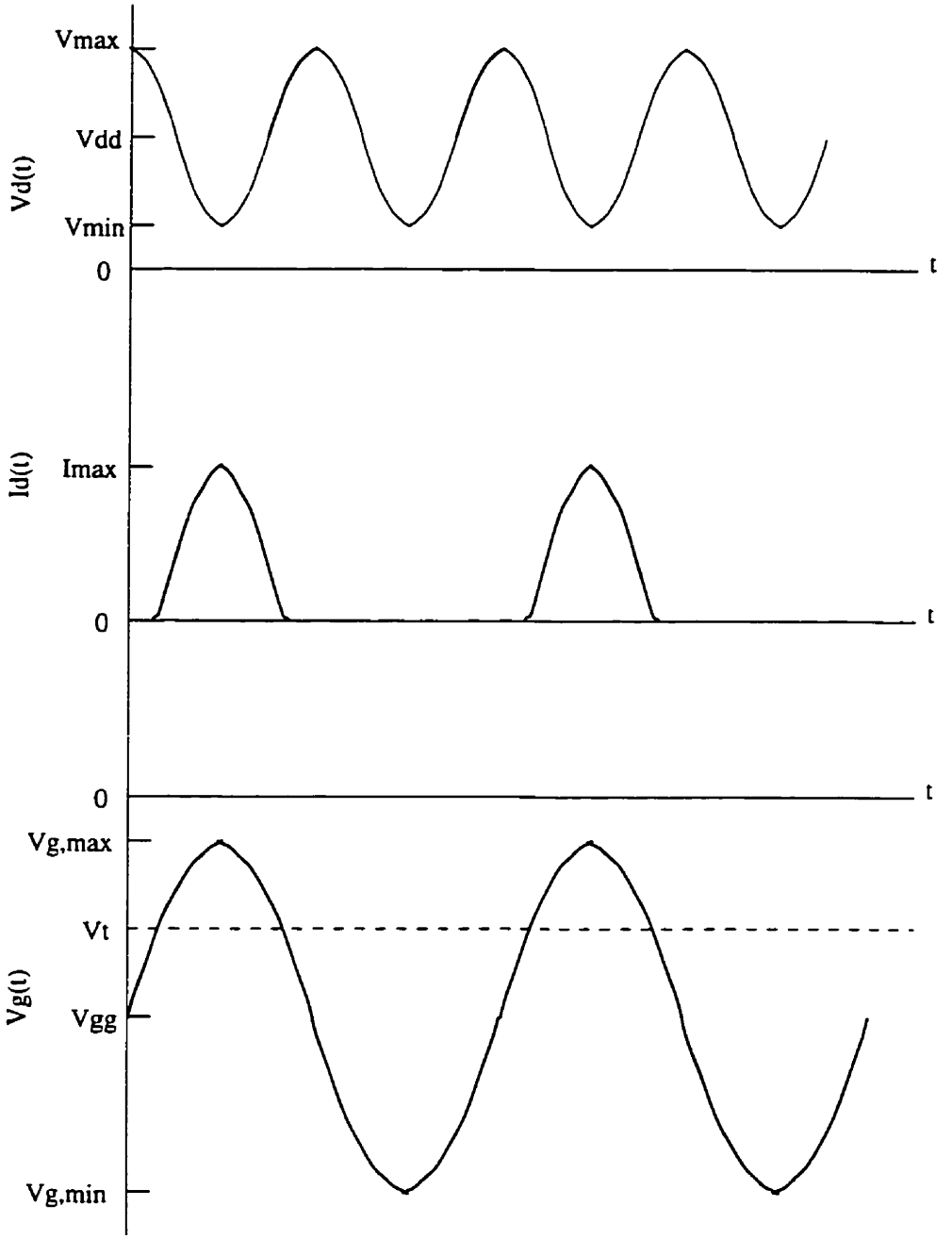


Figure 4.8 Voltage and current waveforms for an ideal FET multiplier.

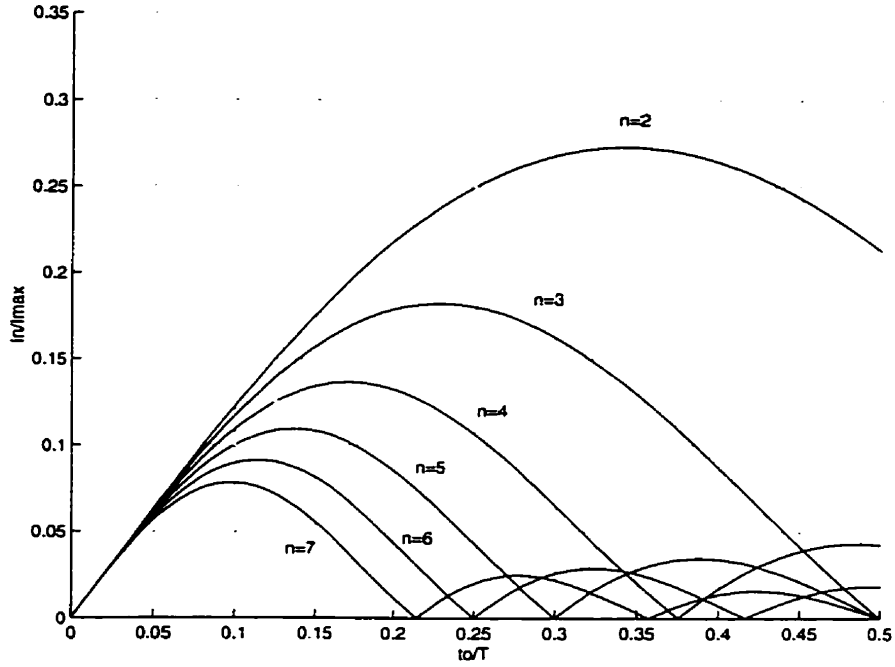


Figure 4.9 Ideal harmonic drain current as a function of FET drain conduction angle.

angle can be obtained using a Fourier series expansion for an ideal cosine pulse train as [36]

$$I_n = I_{max}\frac{4t_o}{\pi T}\left|\frac{\cos(n\pi t_o/T)}{1-(2nt_o/T)^2}\right|, \tag{4.20}$$

where I_n is the drain current for the nth harmonic, I_{max} is the peak drain current, and t_o/T is the conduction fraction of the input period. The harmonic drain current relative to the peak drain current from Equation 4.20 is plotted in Figure 4.9, as a function of t_o/T, for harmonics up to the 7th.

In order to maximize the desired output harmonic, I_n must be maximized. The only degree of freedom for doing this, according to Equation 4.20, is by varying t_o/T. Unfortunately, the conduction angle necessary for optimizing the desired harmonic drain current is quite small, and likely not realizable in a practical FET multiplier, especially for harmonics greater than the 2nd [36]. In order to obtain a small conduction angle, and simultaneously maintain

high peak drain current, the gate bias voltage must be reduced while the input level is increased. If $V_{gg} << V_t$, this operation can result in high peak drain-gate voltages, that may exceed the avalanche voltage of the FET [36], or at the very least, cause instability in the FET [26]. This is the reason that the FET conduction angle cannot be made arbitrarily small. As a result, a non-optimal FET conduction angle must often be chosen to obtain a stable FET operating point.

High Harmonic FET Multipliers

Most published FET frequency multipliers have been doublers [36][37][38][39] due to the difficulty in obtaining the optimum FET conduction angles required in higher harmonic multipliers. However, high harmonic multipliers (multipliers of 4th order or higher) are very attractive, and result in simpler microwave hardware requiring a single FET stage. Multiplication factors as high as $\times 7$ are generally feasible using a single stage FET topology. Higher order FET multipliers can also be designed using a cascade of doublers or triplers, but the hardware complexity increases dramatically as a result of complicated interstage matching and filtering to remove undesired harmonic components. A fifth harmonic multiplier is proposed in this thesis [26].

The optimum FET conduction angle for a $\times 5$ harmonic frequency multiplier is difficult to achieve due to the high reverse gate bias required to achieve such a conduction angle. Therefore, the multiplier is designed to obtain a FET conduction angle corresponding to the second peak in the harmonic drain current versus conduction angle characteristic. From Figure 4.9, the second peak of the fifth harmonic drain current corresponds to a conduction angle of $\frac{t_\theta}{T} = 0.39$ or approximately 140 degrees.

A desirable property of most frequency multipliers is that they be operated in gain saturation, such that slight variations in input signal level are not transferred to the output (ideal "hardlimiter" function). As with

power amplifiers [36], this requires that the harmonic load current generate the maximum load voltage variation permitted by the FET I-V curves [36]

$$|V_L(t)| = I_n R_L = \frac{(V_{max} - V_{min})}{2}, \tag{4.21}$$

where I_n is given by Equation 4.20 and is the current in the load resistance, R_L, and V_{min} and V_{max} are the drain voltages shown in Figure 4.8. For saturation, V_{min} should correspond to the I-V "knee" voltage, at the peak of the gate voltage. Equation 4.21 defines the required harmonic load resistance for the saturation condition as

$$R_L = \frac{(V_{max} - V_{min})}{2I_n}. \tag{4.22}$$

Since I_n is small for high harmonic multipliers, Equation 4.22 requires that the harmonic load resistance to be quite large to provide the maximum load voltage swing. This typically results in impractically large load resistances for microwave load matching, and output saturation is not feasible.

A "saturation" condition could be achieved by exploiting the FET conduction angle characteristic, shown in Figure 4.9. That is, if the operating conduction angle is chosen to the right of the conduction angle peak, the reduction in $\frac{I_n}{I_{max}}$, as a function of increasing input level which increases $\frac{t_o}{T}$, could be chosen to offset the increase in I_{max} which occurs with increasing input level. The result of this would be a stabilizing of I_n with increasing input level which would represent a saturation like condition. This phenomenon was not explored in this research, but could be a valuable feature in future multiplier realizations.

The $\times 5$ multiplier, shown in Figure 4.10, consists of a GaAs FET, input and output matching circuitry, output harmonic termination circuitry, and biasing circuitry (not shown in Figure 4.10). The multiplier is designed by

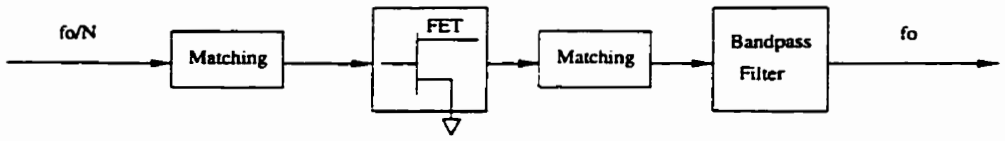


Figure 4.10 Functional block diagram of frequency/phase multiplier.

selecting a gate input level and bias point to obtain a conduction angle corresponding to the second peak in the 5th harmonic conduction angle equation. The gate bias point, however, must also be selected to maintain unconditional stability in the FET at the fundamental and all harmonic frequencies present in the multiplier. Unconditional stability is not a necessity, but is a practical requirement, considering the difficultly in controlling the circuit source and load impedances to be at stable points for all frequencies. Input matching circuitry is designed to conjugately match the phase shifter output impedance to the low gate impedance of the FET at the subharmonic input frequency. As the input impedance of the FET is essentially reactive, wideband input matching is very difficult. The FET input matching is a limiting factor in the design of a wideband phase shifter with acceptable amplitude modulation (AM) performance. A poor match between the phase shifter output and the frequency multiplier input results in signal level variation as a function of the phase control voltage. Fortunately, this effect is mitigated by the increase in effective output bandwidth by a factor of $\times N$ as a result of frequency multiplication, so narrowband subharmonic gate matching is usually acceptable. Input and output matching circuitry is designed to provide simultaneous conjugate match at the fundamental frequency on the input, to preserve the desired gate conduction angle, and at the harmonic frequency on the output, to maximize the harmonic output level. The use of nonlinear microwave simulation software such as HP-EEsof Libra© can prove very useful for this purpose. A narrowband bandpass filter (BPF) is required on the output to reject all unwanted harmonic signals and provide the desired harmonic termination impedances to the FET drain.

4.3 Summary

This chapter described some of the critical considerations in design of the direct microwave GMSK modulator hardware. The fractional phase shifter is designed as a 3 dB quadrature hybrid coupler, with through and coupled ports terminated in reactive varactor controlled reflective terminations. The termination reactance must be matched to the ideal sliding short circuit reactance tangent function, to obtain highly linear phase control. A hyperabrupt junction varactor may provide better match to the tangent function than an abrupt junction varactor, if the varactor parasitic package capacitance is significant. The frequency/phase multiplier provides an output signal at the 5th harmonic frequency of the phase shifter output signal. It also expands the linear phase shift range of the fractional range shifter by a factor of $\times 5$. The multiplier is designed by selecting an unconditionally stable Class C bias point and gate input level to obtain a FET conduction angle conducive to high 5th harmonic output. The input and output of the FET are matched to provide conjugate matching at the fundamental frequency at the input and at the 5th harmonic frequency on the output, while terminating the output drain appropriately for unwanted harmonics.

Chapter 5 further expands on these design equations, and provides detailed implementation concerns and microwave simulation results.

5. DIRECT GMSK MODULATOR REALIZATION

This chapter expands on the direct GMSK modulator design parameters explored in Chapter 4 to present detailed microwave circuit realizations for the modulator. Fabrication and implementation concerns for microwave circuits at 18 GHz are discussed, and simulation results using HP-EEsof Series IV© [43] microwave design software are presented. These simulation results are useful for confirming some of the mathematical results presented in Chapter 4, and for direct comparison to measured results of the fabricated circuits presented in Chapter 6.

5.1 Fabrication Technology

Microwave integrated circuit (MIC) fabrication techniques were used for realization of the prototype modulator circuits. This technology is a fast and relatively inexpensive method of fabricating a prototype microwave or millimeter-wave circuit. The MIC circuits are planar microstrip circuits, with the metal microstrip conductors deposited on a low-loss dielectric substrate using thin-film technology. Lumped element resistors and capacitors can also be deposited on the substrate using thin film technology, or the lumped element components can be attached directly to the microstrip lines using the appropriate solder or conductive epoxy. The latter option was chosen for the lumped elements, to reduce the cost of fabrication for this prototype implementation.

Monolithic microwave integrated circuit (MMIC) technology could also be used to implement the planar modulator circuits. An MMIC is a planar

microwave or millimeter-wave circuit in which the active and passive circuits structures are fabricated using a common semiconductor substrate. The initial prototype circuit fabrication cost to design an MMIC is extremely high. The principle advantage in using MMICs is that the cost becomes very low if the circuits are manufactured in large quantities.

5.1.1 Substrate

Microwave substrate materials must have constant relative permittivity, ϵ_r, with temperature and frequency, and low dielectric loss tangent, $\tan\delta_\epsilon$. Copper-clad glass fibre reinforced plastic laminates have these desirable properties and are very popular substrate materials for MIC implementation at lower microwave frequencies. The reason for this popularity is that plastic laminates are inexpensive, easy to fabricate using a simple photoetching process, and easy to machine. At frequencies greater than 10 GHz, plastic laminates are less suitable due to high dielectric losses and parasitic transverse resonance modes [44].

Ceramic substrates are also commonly used at microwave and millimeter-wave frequencies. The most common of these is aluminum-oxide (Al_2O_3), which is also called "alumina". Alumina has higher relative permittivity (ϵ_r of 9.8 - 9.9, typically) than plastic laminates (ϵ_r of 2-3, typically), which allows for reduced circuit geometries and higher levels of circuit integration. In packaged circuits, smaller geometries are also of benefit as the cut-off frequencies of package resonant modes are increased. Alumina has a very low loss tangent ($\tan\delta_\epsilon$=0.0001 at 10 GHz) and is a suitable substrate material for microstrip MIC implementation at frequencies up to 30 GHz [44].

The disadvantage in using alumina is that it requires expensive thin film fabrication techniques. The substrate is metalized in gold by sputter deposition [45], to provide very thin microstrip conductors ($2-4\mu$m typically). This process of "pattern plate-up" as opposed to etching is capable of achieving

very small geometries (10μm typical line widths and spacings). Alumina is also very brittle, and cannot be easily machined. Holes and cuts are normally laser drilled.

Despite the increased fabrication complexity, alumina was chosen as the substrate for implementation of the prototype circuits, due to its superior electrical properties at upper microwave frequency, when compared to plastic laminates. The 3.6 GHz portion of the circuitry could have been implemented using plastic laminate, but was also implemented on alumina, for consistency. The chosen substrate is 99.6% pure Al_2O_3, with $\epsilon_r = 9.9$, substrate thickness of 25 mil, and conductor thickness of 0.15 mil. The physical substrate parameters corresponding to various transmission line parameters for this substrate can be calculated using the Series IV LineCalc program [43]. The microstrip line width for a 50 Ω transmission line is 25 mil. The $\lambda/4$ line length ($\pi/2$ radian electrical length) at a frequency of 3.6 GHz is 320 mil. and at 18 GHz is 60 mil.

5.2 Fractional Phase Shifter

The schematic diagram with microstrip conductor pattern for the fractional phase shifter implementation at 3.6 GHz is shown in Figure 5.1. The circuit designators are also listed in Figure 5.1. This schematic is referred to throughout this section, as various parts of the phase shifter design are described in detail.

5.2.1 Hybrid Coupler

The quadrature hybrid coupler, H1, is shown in Figure 5.1. The widths and lengths of the through and coupled paths were first calculated using LineCalc to provide a starting point for the required electrical characteristics at an input frequency of 3.6 GHz, as described in Section 4.1.1. A frequency sweep was done on the 4-port network using a Linear Test Bench [43], with

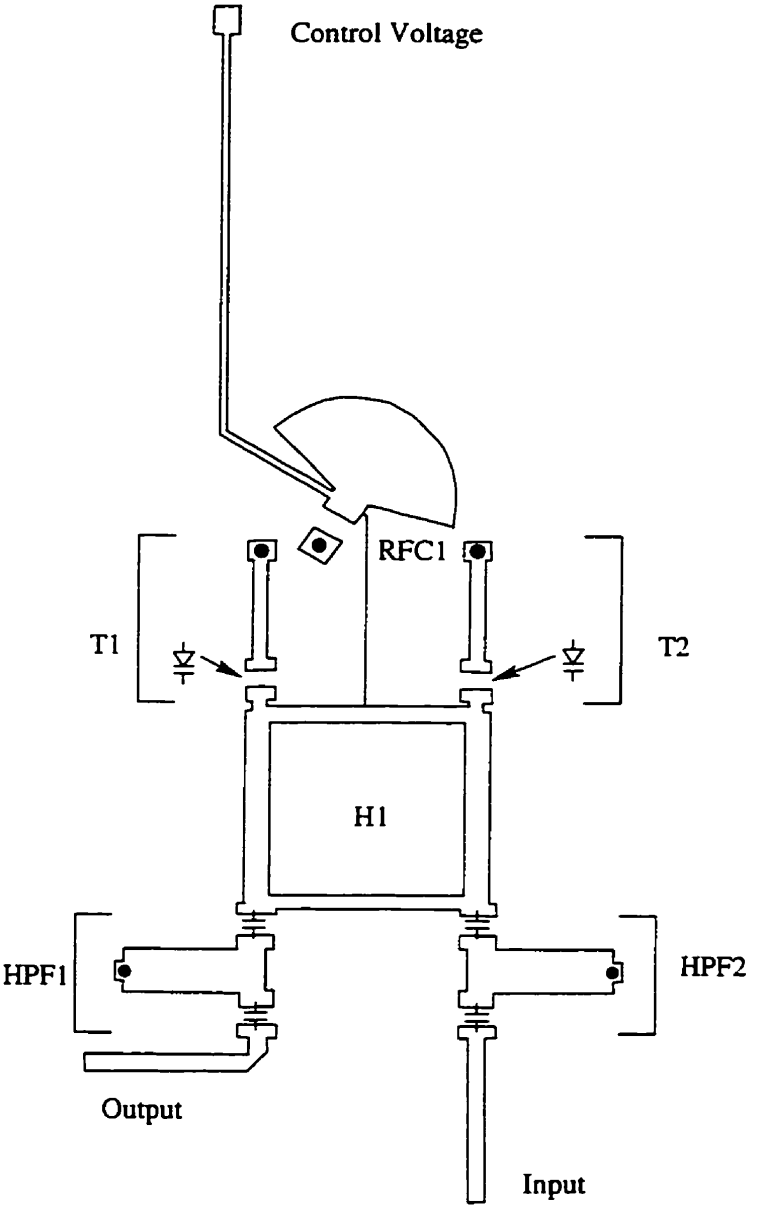


Figure 5.1 Microstrip schematic of the fractional phase shifter.

the through and coupled ports of the hybrid terminated in 50 Ω. Initially, the input match was a bit lower than 3.6 GHz, so the circuit dimensions were optimized to obtain a good input match centred at 3.6 GHz and good amplitude and phase balance at the through and coupled ports. This optimization yielded a 3 dB, 90 degree coupler with an input return loss of > 26 dB, amplitude balance of ±0.1 dB, and phase balance of ±0.1 degree over a 200 MHz bandwidth at 3.6 GHz.

5.2.2 Reactive Terminations

Reactive terminations, T1 and T2, were designed based on a grounded series combination of inductance and varactor capacitance, as described in Section 4.1.2. In Section 4.1.2, it was determined that at an operating frequency of 3.6 GHz, a hyperabrupt junction varactor, with $\gamma = 0.75$, provided a better match to the reactance tangent function and more linear phase shift through the reflection phase shifter than an abrupt junction varactor. Varactor diodes are available in both GaAs and silicon. The Q of GaAs hyperabrupt varactor diodes is typically 5 to 6 times higher [34] than that of silicon, which makes GaAs a better choice for a low loss reflective termination at 3.6 GHz. An M/A-Com MA46H071-1056 surface mount GaAs tuning varactor [46] is an appropriate varactor, and was chosen for this application. It has a maximum capacitance, $C_o = 2.4$ pF, a Q> 60 at 3.6 GHz and parasitic series resistance $R_s < 2\ \Omega$ over the bias voltage range, package capacitance of 0.15 pF, and series package inductance of 0.45 nH. The minimum varactor capacitance, C_{min}, is 0.46 pF and corresponds to $V_N = 1$, or $V_R = 10.5$ V, where $\Phi = 1.3$ V for GaAs. These varactor parameters were used in the model shown in Figure 4.3. This model was implemented in Series IV, with the variable capacitance versus voltage relationship defined as in Equation 4.12. Reverse voltage was also configured as a linear sweep variable, so the circuit could be simulated as a function of reverse bias voltage.

The total series inductance required for optimal match to the reactance tangent function at 3.6 GHz was determined in Section 4.1.2 as $L_s = 3.54$ nH. Therefore, including the parasitic package inductance, 3.09 nH of additional series inductance is required in the terminations. Another source of parasitic inductance in the series termination is the metalized via hole in the substrate required to connect the varactor anode to the ground plane. The via was modelled in Series IV as a series RL circuit. The resistance at 3.6 GHz is negligible but the parasitic inductance of the via is on the order of 0.1 nH for a 25 mil. diameter metalized via hole in a 25 mil. substrate, which is significant when compared to the desired series inductance.

The remaining series inductive reactance can be realized using either printed or lumped elements. A lumped-circuit element is generally considered to be one in which its physical dimensions are much smaller than the operating wavelength, and therefore, does not exhibit appreciable distributed phase shift effects. Surface mount chip inductors generally have self resonant frequencies and Q values which are too low to be useful at 3.6 GHz. Lumped element inductors suitable for microwave frequencies can be realized as pieces of metallic ribbon or wire or as circular or rectangular printed spirals [47]. Ribbons and wires are typically useful for realizing inductance values up to 2-3 nH [47]. In this application, accurate inductance values are required for maximum phase shift linearity. Difficulties in accurately modelling the inductance, controlling the length and shape, and connecting the wires or ribbons, excluded this method from consideration for the prototype.

Printed transmission line spirals are used to realize inductors with high Q (typically > 80 at 4 GHz [47]) and high inductance values (up to 20 nH at 4 GHz [47]). As a result of the magnetic coupling between the transmission lines, these inductors are substantially smaller than the straight wire type and are often used for high density circuits such as MMICs. The number of turns, transmission line width, transmission line spacing, and the distance

above the ground plane, all affect the inductance value, self-resonant frequency, and Q of the printed inductor [47]. One drawback in using printed spirals is that connection to the inside of the spiral must be made using either an air-bridge [44] or bond wire, which makes these more difficult to implement in planar microwave circuitry. In this application, the inductor is grounded, so a metalized via to ground could be put inside of the printed spiral, removing the need to connect to the inside of the spiral with an air-bride or wire. Printed spiral and rectangular inductors were simulated in Series IV. In order to get the desired inductance values, and maintain small lumped element dimensions to avoid distributed effects, the inside diameter of the spiral became too small to enclose a via with the minimum diameter via hole permitted by the chosen laser drilling process. Therefore, since an air-bridge or wire was still required to connect to the inside of the spiral, this approach was abandoned.

Purely reactive circuit elements can also be realized by using open or short circuited microstrip transmission lines, of appropriate length and characteristic impedance. The varactor diode must be DC biased, thus, a shorted transmission line is easier to implement than an open as it provides a DC path to ground without the need for an additional RF choke. The input impedance of a lossless short circuited transmission line is given by

$$Z_{sc} = jZ_o \tan\theta, \tag{5.1}$$

where Z_o is the characteristic impedance of the line and $\theta = \frac{2\pi l}{\lambda}$ is the electrical length of the transmission line. From Equation 5.1, it is apparent that a lossless short circuit transmission line is a purely reactive element, with reactance that varies along the transmission line. As one moves away from the short circuit, the reactance changes from a short, through inductive values, to an open (at distance multiplies of $\lambda/4$), through capacitive values, and back

to a short (at distance multiplies of $\lambda/2$). If the length of the transmission line is $\lambda/8$ at the operating frequency, f_o, then $\tan\theta = 1$ and $Z_{sc} = jZ_o$, which is equivalent to a lumped inductive reactance of $Z_{ind} = j2\pi f_o L$, if Z_o is set equal to $2\pi f_o L$. Equation 5.1 can be written to reflect the change in short circuit line reactance as a function of frequency as

$$Z_{sc} = jZ_o \tan\frac{\pi f}{4f_o}. \tag{5.2}$$

At the centre frequency, f_o, the transmission line inductive reactive, Z_{sc}, equals the lumped element equivalent inductive reactance, Z_{ind}. As the frequency deviates from f_o, Z_{sc} deviates from Z_{ind}, but for narrowband circuits. Z_{sc} is a good approximation for Z_{ind}. For example, over a 10% bandwidth, Z_{sc} is typically within $\pm 3\%$ of Z_{ind}.

Therefore, one would expect that the performance of the phase shifter with the transmission line inductive reactance termination to be comparable to the lumped inductive reactance termination at the centre frequency, and deviate slightly from the performance of the lumped inductive termination as a function of frequency. The termination reactance as a function of frequency is not of major concern in this application, as the input signal to the reflective terminations is a CW signal and the termination characteristic has been optimized for maximum phase shift linearity performance at a single frequency.

As a starting point in Series IV, a $\lambda/8$ line at 3.6 GHz, with characteristic impedance of $Z_o = 2\pi(3.6)(3.09) = 69.9\ \Omega$, was shorted to ground using the via model. The dimensions of the line were then optimized to provide an overall input impedance of $j69.9\ \Omega$ at 3.6 GHz. A short microstrip line was also required to connect the varactor cathode to the coupler ports, and provide a suitable bonding area for the varactor. If the length of this pad is kept as short as possible, the impact on the reactive termination phase

shift linearity with bias is negligible. As the line occurs before the variable reactance portion of the reactive termination, it represents only a constant phase offset in the reflection coefficient phase.

A Series IV simulation was done to evaluate the effectiveness of the reactive termination realization. The phase of the termination reflection coefficient was measured as a function of the varactor reverse bias control voltage, at a CW input frequency of 3.6 GHz. Figure 5.2 shows the reflection coefficient phase in degrees as a function of reverse bias voltage. A total change in the reflection coefficient phase of 82 degrees is obtained over a bias range of 0 to 10 V. The phase control range agrees with that estimated in the mathematical simulation in Section 4.1.2. The reflection coefficient phase linearity, in radians, as a function of reverse bias voltage is shown in Figure 5.3. The phase distortion of 0.00876 radians over a bias range of 0 to 10 V corresponds to ± 0.25 degrees, and is also comparable to the calculated values in Section 4.1.2. These results verify the mathematical calculations in Section 4.1.2, and lend confidence to the feasibility of the termination realization method.

5.2.3 RF Choke

The varactor diodes must be biased with DC signals for a phase shifter, or baseband modulation signals for a phase modulator, without adversely affecting the phase shifter performance at the operating frequency of 3.6 GHz. In other words, the baseband signals must be injected into the phase shifter and appear across the varactors without loading the shifter at 3.6 GHz. This requires that the baseband feedline present a high impedance to the phase shifter circuit at 3.6 GHz. This feedline is often termed an "RF choke".

Lumped inductors are often used as RF chokes at lower frequencies. At microwave frequencies, it is difficult to design large value lumped inductors,

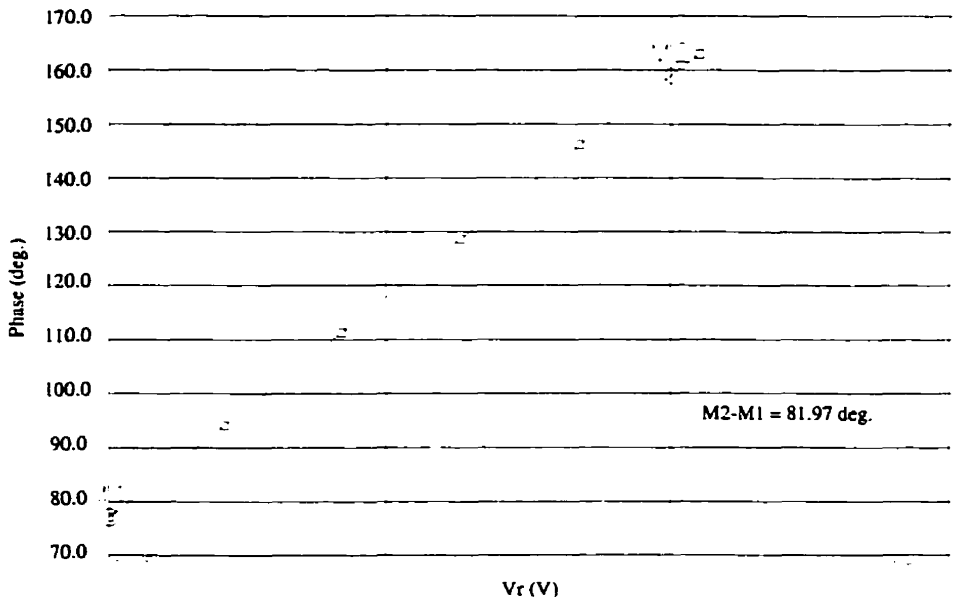


Figure 5.2 Simulated reactive termination reflection coefficient phase as a function of reverse biased varactor voltage.

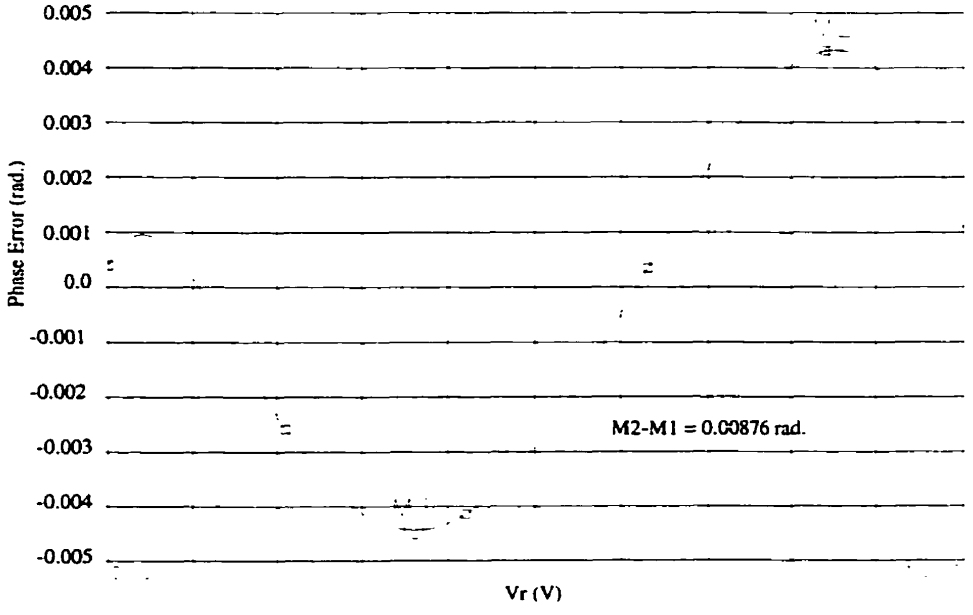


Figure 5.3 Simulated reactive termination reflection coefficient phase shift linearity as a function of reverse biased varactor voltage.

and most RF chokes are realized using high impedance microstrip lines. At lower microwave frequencies, large value chip resistors are sometimes used as wideband RF chokes for DC biasing applications where negligible current draw is required, as in the case of FET gate biasing. As the phase shifter application is not restricted to DC biasing, but is designed to function with baseband modulation, a large value resistor is inappropriate and would dramatically limit the baseband bandwidth in combination with the varactor capacitance.

A single microstrip printed choke is used to simultaneously bias both varactors. The choke, RFC1, consists of a high impedance $\lambda/4$ line at 3.6 GHz and a microstrip radial stub. The radial stub provides a short circuit at 3.6 GHz, which is transformed to an open circuit at the coupler tap point by the $\lambda/4$ line. An open circuit $\lambda/4$ line could also be used to realize the microwave short circuit. The radial stub is an attractive option, however, as it is tends to be more compact than the open circuit $\lambda/4$ line. Provision was also made on the choke to add a chip capacitor at the short circuit point, if required to improve the choke. Inclusion of the capacitor limits the baseband bandwidth, as it is in parallel with the varactors and increases the load capacitance to the baseband driving signal. A good microwave short circuit is critical at the end of the choke $\lambda/4$ line. This is because the baseband signal feedline, connected to the short point, provides an unpredictable impedance at microwave frequency. The impedance of this feedline is not critical if in parallel with a good microwave short.

5.2.4 Baseband Signal Rejection

The baseband signal must be contained in the phase modulator, and effectively blocked from escaping through the input or output ports. If the baseband modulating signal is restricted to DC, the signal can be blocked using relatively high value series capacitors on the input and output, which

provide a low reactance path to the microwave signals. With baseband modulation signals, there is not adequate rejection using a single blocking capacitor to permit high frequency baseband modulation, unless the blocking capacitor is reduced to a very small capacitance value. In this situation, the small value blocking capacitors are no longer low reactance at microwave frequency, and input and output matching circuits must be added to match this series reactance to 50 Ω. This matching operation unnecessarily reduces the operating bandwidth of the circuit.

A better solution to the blocking problem for wideband baseband modulation is provided using filters on the phase modulator input and output. The filters are designed to have 50 Ω impedance in the passband, removing the requirement for complicated input and output matching circuitry. Both bandpass and highpass filters are appropriate for rejecting the baseband modulation signals. The filter order is chosen high enough to provide the desired rejection at the maximum baseband signal frequency. An added advantage of bandpass filters is that they also reject unwanted harmonic modulation signals, which may be generated by large-signal nonlinearities in the termination varactors. Bandpass filters also tend to have higher passband loss than highpass filters, so the overall loss in the phase modulator would be expected to increase.

Highpass filters, HPF1 and HPF2, were chosen for this implementation. The normalized lumped elements for a 3rd order Butterworth highpass filter [33] are $R_s = R_L = C_1 = C_3 = 1$, and $L_2 = 0.5$. These elements are for a T-equivalent circuit with two series capacitors around a shunt inductor. The Butterworth filter response was chosen as it provides reasonably good selectivity while maintaining low amplitude and phase distortion characteristics, provided that the passband is not too close to the cut-off frequency. It is difficult to transform the lumped element highpass filter to a distributed microwave filter due to the absence of a convenient distributed series capacitor

equivalence [48]. As a result, most highpass filters at microwave frequency are designed as a combination of lumped capacitors and distributed inductors [48]. Also, true highpass filters are difficult to design at microwave frequencies, and tend to roll off as the frequency increases, due to parasitics in lumped elements and the narrowband nature of distributed elements. As a result, most microwave highpass filters are actually bandpass filters and only approximate the highpass characteristic around the cut-off, and deviate from this characteristic as the frequency is increased. These filters also tend to be reentrant at some higher harmonic frequencies, due to the use of distributed elements [48], meaning that they have multiple passbands.

The highpass filter is realized using high Q porcelain microwave chip capacitors for the series capacitor elements and a shorted stub for the inductor element. The normalized circuit values are impedance and frequency scaled as [33]

$$C' = \frac{C}{R_o \omega_c}, \tag{5.3}$$

$$L' = \frac{L R_o}{\omega_c}, \tag{5.4}$$

where L and C are the normalized element values listed above, R_o is the source resistance, and ω_c is the desired cut-off frequency. The inductive reactance is realized using a shorted stub. From Equation 5.1, it was shown that a $\lambda/8$ line provided $Z_{sc} = jZ_o$. Equation 5.4 shows that the desired inductive reactance at ω_c is $LR_o = 0.5(50) = 25\ \Omega$. Therefore, a shorted 25 Ω microstrip line that is $\lambda/8$ at the cut-off frequency provides a distributed equivalent inductance.

Series capacitors of 1.4 pF provide a highpass cutoff frequency of 2.27 GHz, far enough below the passband of 3.6 GHz to provide low amplitude and phase distortion. The $\lambda/8$ line length at 2.27 GHz is approximately 220

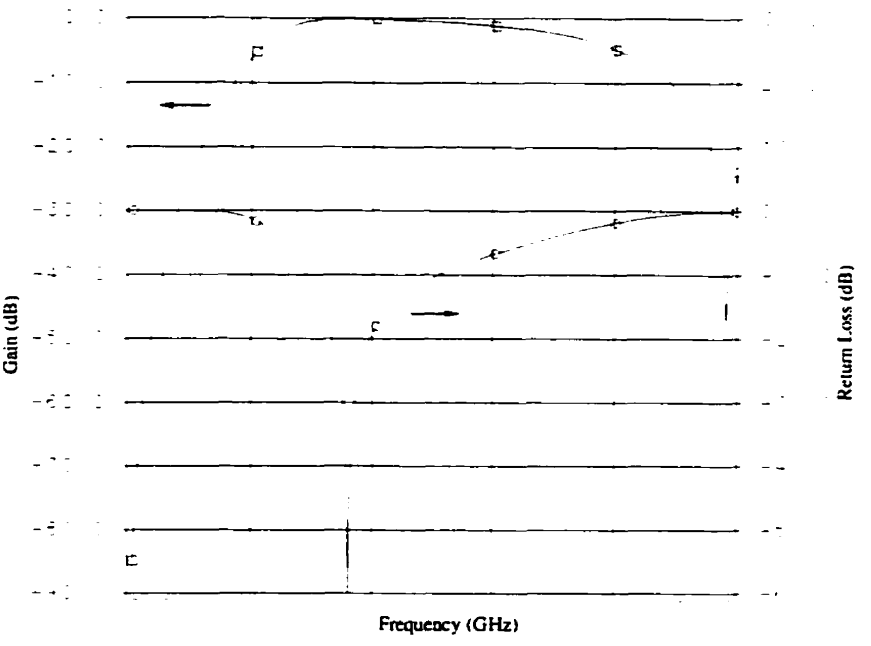


Figure 5.4 Highpass filter amplitude response and return loss.

mil. The transmission line dimensions were optimized to provide the desired passband characteristics for the highpass filter. The highpass filter amplitude response and return loss is shown in Figure 5.4, where the arrows in the figure indicate the appropriate axis for the responses. The return loss is tuned to be optimum at a passband frequency of 3.6 GHz. As expected, the highpass filter is actually bandpass, due to distributed element and parasitic component effects. The passband amplitude and phase distortion over 1 GHz are shown in Figure 5.5 and Figure 5.6, indicating that the input and output filters contribute little distortion to the bandpass signal. The parabolic shaped passband phase distortion shown in Figure 5.6, actually improves the overall phase shifter phase distortion, since the inherent phase shifter distortion is parabolic in the opposite sense. Therefore, the cascade of two stages of highpass filters reduces the overall phase distortion. The highpass filters provide a rejection of > 30 dB up to 700 MHz and are adequate for wideband baseband modulation.

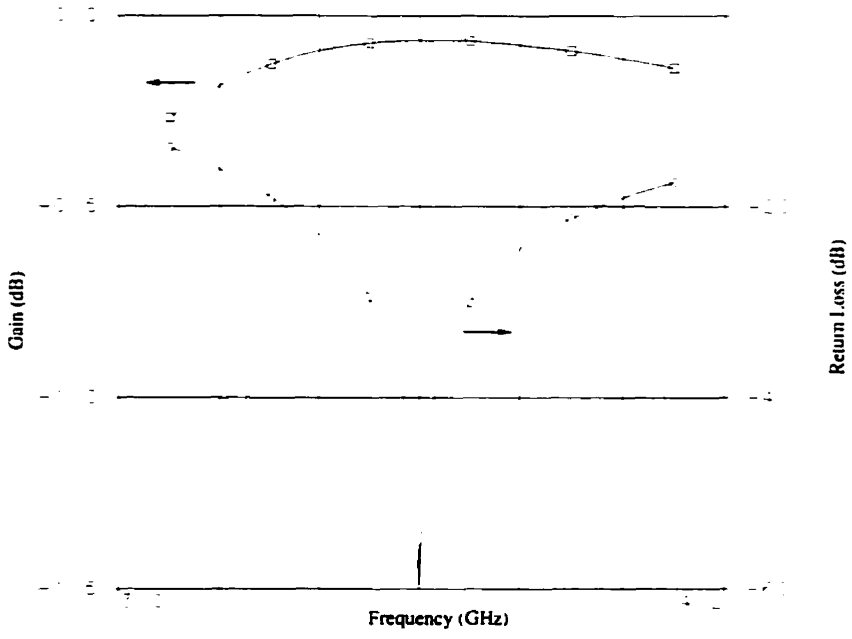


Figure 5.5 Highpass filter passband amplitude distortion and return loss.

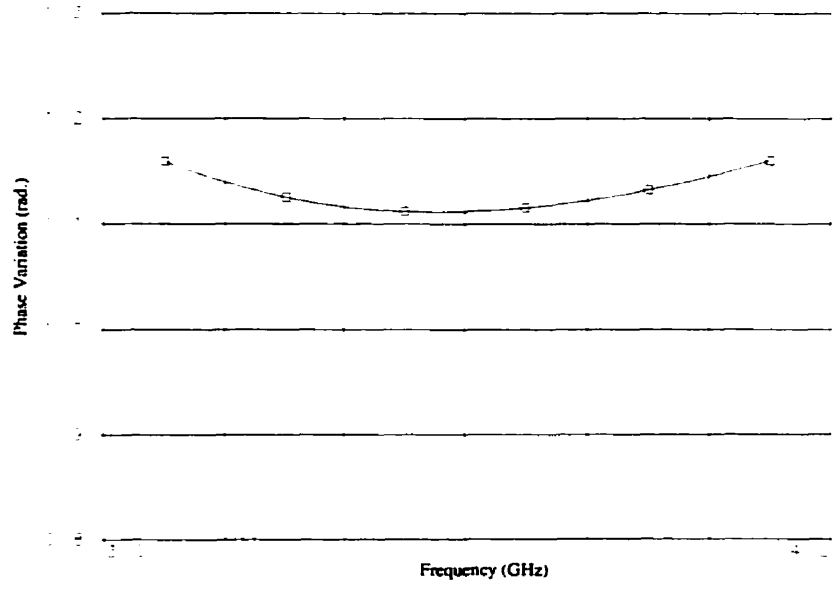


Figure 5.6 Highpass filter passband phase distortion.

5.2.5 Simulation Results

The fractional phase shifter circuit was simulated using HP-EEsof Libra Software to assess the performance as a function of frequency, with fixed bias, and as a function of bias, with fixed frequency.

Figures 5.7 and 5.8 show the fractional phase shifter amplitude response ($|S_{21}|$) and return loss ($|S_{11}|$) as a function of frequency for several reverse bias voltages. Figure 5.9 shows the fractional phase shifter phase distortion as a function of frequency, which is worst case for a 0 V reverse bias. Figures 5.7 to 5.9 demonstrate that the phase shifter is quite wideband in nature. The useful output bandwidth at 3.6 GHz is about 600 MHz, with amplitude and phase distortion within 0.5 dB and 6 degrees, respectively, and return loss better than 10 dB across the band. There is also very little loss through the phase shifter (0.5 to 1.5 dB at 1.3 V as shown in Figure 5.7) which suggests a high Q implementation, with the parasitic termination resistance contributing very little to the circuit loss. The phase shifter performance as a function of frequency is not as important for this application as the performance as a function of bias voltage, as the input to the shifter is a CW not a wideband signal and, therefore, only a CW signal is input to the reflective terminations. The good performance as a function of frequency, however, is encouraging as it suggests that the phase shifter will support high rate modulation, independent of the varactor modulation bandwidth.

The fractional phase shifter phase shift and gain at 3.6 GHz, as a function of bias voltage, is shown in Figure 5.10. The phase shift linearity as a function of bias at an operating frequency of 3.6 GHz is shown in Figure 5.11. From Figure 5.11, the phase error from linear at 3.6 GHz is 0.0044 radians or 0.25 degrees, over a bias voltage range of 1.3 to 11.3 V. From Figure 5.10, this same bias voltage range corresponds to a phase shift of 78.5 degrees. The amplitude variation over the bias range was quite low, and on the order of 0.1 dB.

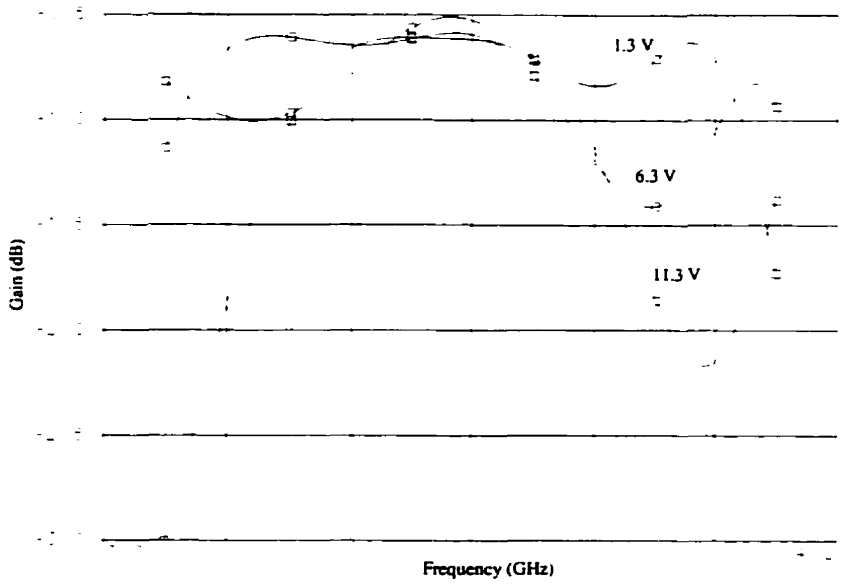


Figure 5.7 Fractional phase shifter amplitude response as a function of frequency for several bias voltages.

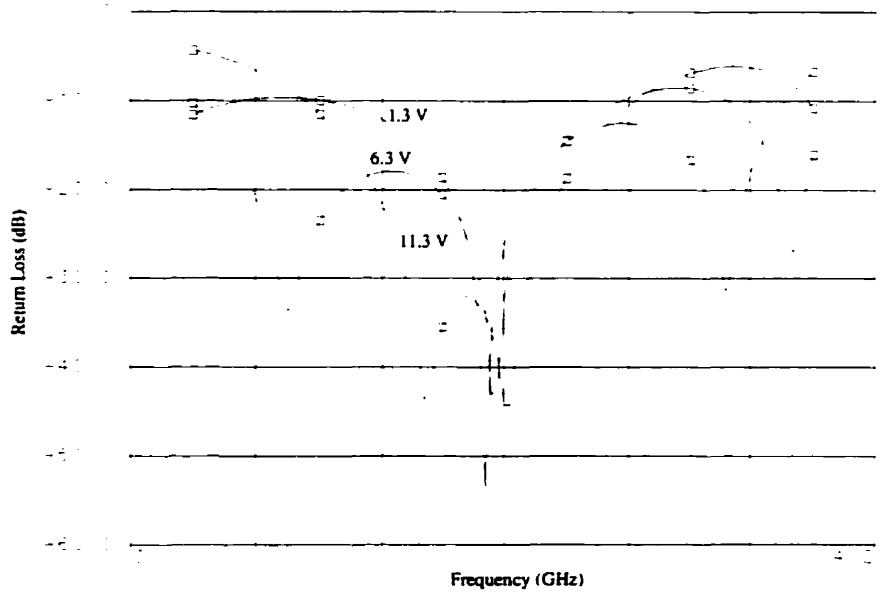


Figure 5.8 Fractional phase shifter return loss as a function of frequency for several bias voltages.

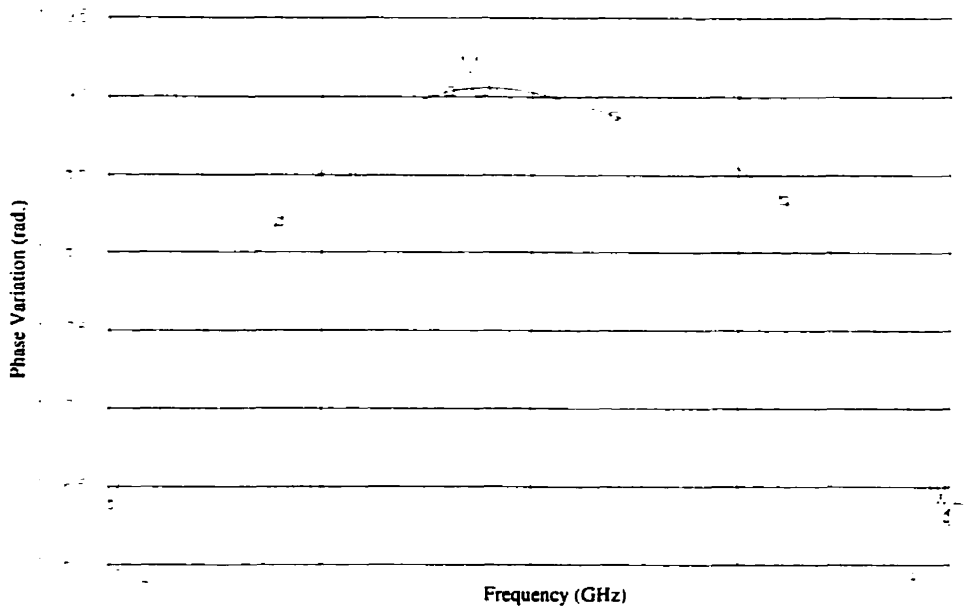


Figure 5.9 Fractional phase shifter phase distortion as a function of frequency for a bias voltage of 0 V.

These simulation results as a function of bias suggest a very high performance phase shifter with low residual AM, providing linear phase shift of a microwave carrier signal at 3.6 GHz over an adequate phase shift range for this application. The simulated phase shift range and linearity for the phase shifter at 3.6 GHz is also comparable to the simulation of the terminations in Figures 5.2 and 5.3 and to the mathematical calculations of the termination characteristics in Section 4.1.2. This provides much confidence in the validity of the phase shifter design and in the method of realizing practical terminations with reactance having a good match to the desired tangent function. The next section provides detailed information on the microwave realization of the frequency/phase multiplier.

5.3 FET Frequency/Phase Multiplier

The schematic diagram with microstrip conductor pattern for the $\times 5$ frequency/phase multiplier implementation at 18 GHz is shown in Figure 5.12. The circuit designators are also listed in Figure 5.12. This schematic is re-

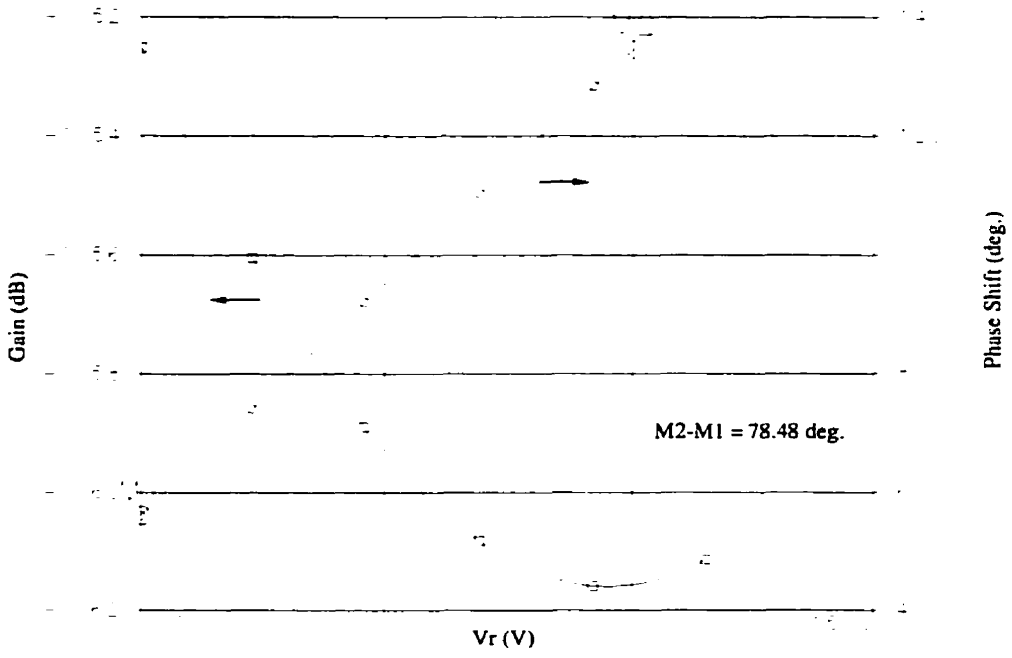


Figure 5.10 Fractional phase shifter phase shift and gain as a function of bias voltage at 3.6 GHz.

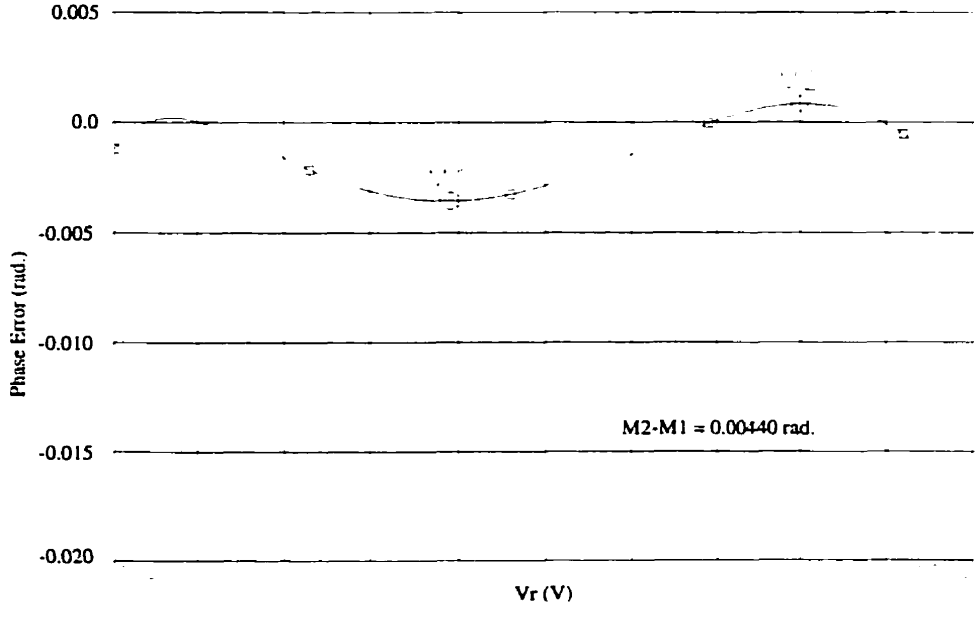


Figure 5.11 Fractional phase shifter phase shift linearity as a function of bias voltage at 3.6 GHz.

ferred to throughout this section, as various parts of the multiplier design are described in detail.

The frequency/phase multiplier nonlinear circuit behaviour was simulated using nonlinear analysis in Series IV [43]. Series IV uses the Harmonic Balance method [36], which allows analysis of circuits containing both linear and nonlinear elements excited by large-signal periodic sources [43]. Harmonic Balance is a powerful method for analyzing strongly nonlinear circuits having single-tone excitation [36], of which the FET multiplier presented in the thesis is an example. The validity of the Series IV software in accurately performing Harmonic Balance for effective nonlinear analysis was taken on faith. The Harmonic Balance method is not presented in detail in this thesis, and the reader is referred to Maas [36] for a comprehensive discussion of the technique.

The Harmonic Balance method is based on the assumption that for a sinusoidal excitation, there exists a steady state solution for the network node voltages and currents that can be approximated using a Fourier series. This solution can be represented as a set of node voltage and current phasors at harmonics of the fundamental excitation frequency. Therefore, the accuracy of the approximation of the steady state nonlinear behaviour improves as more harmonics of the fundamental excitation are assumed in the analysis. The circuit is divided into linear and nonlinear subcircuit multiport networks, with each element in the nonlinear subcircuit connected to a port in the linear subcircuit. The premise of the Harmonic Balance is that if a set of harmonic port voltages gives the same solution, within acceptable error, for the port currents as calculated in both the linear and nonlinear subnetworks, then these port voltages approximate the steady state solution up to the chosen harmonic with the specified degree of accuracy. The port voltages and corresponding currents for the linear network are calculated first in the frequency domain, using N-port parameter representations and linear circuit

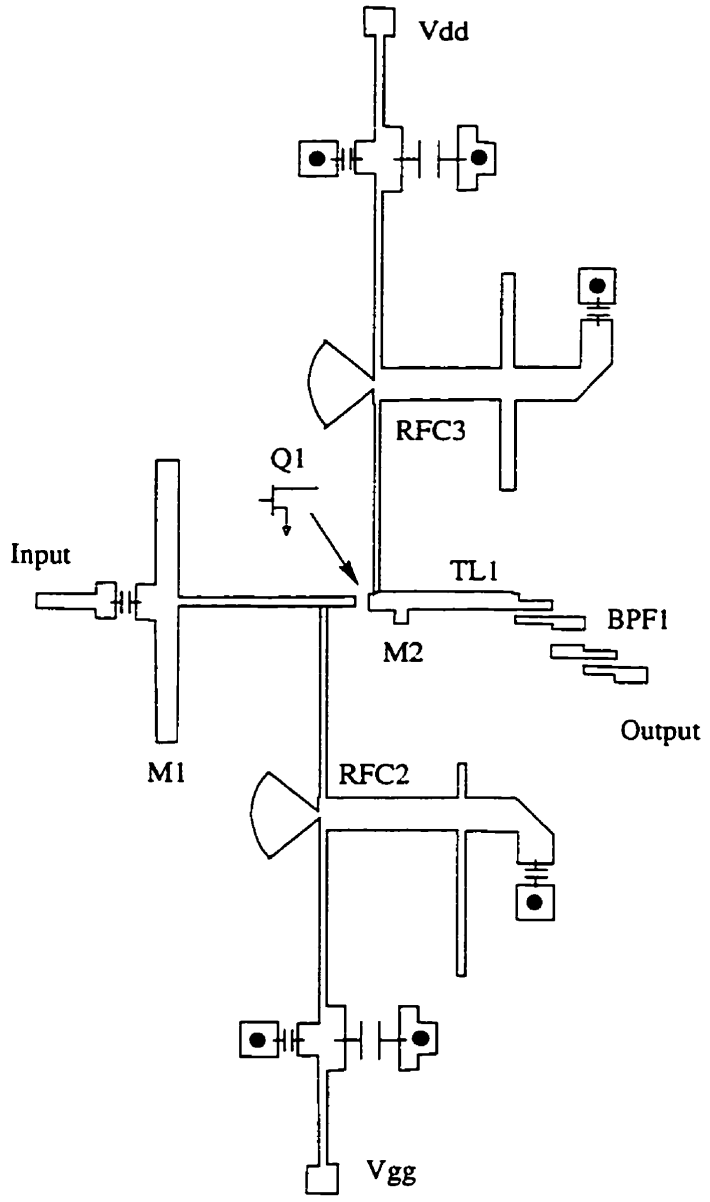


Figure 5.12 Microstrip schematic of the frequency/phase multiplier.

analysis techniques. An inverse Fourier transform is then performed on the port voltages to obtain the port time voltage waveforms. The currents into the nonlinear elements at the ports are then determined from the port voltage time waveforms and the models for the nonlinear elements. A Fourier transform is then performed on the nonlinear port current time waveforms to convert these to the frequency domain, for comparison with the port currents as calculated by the linear subcircuit. This comparison is the basis for an error function meant to drive a new estimate of the port voltages. This process of estimation is repeated until convergence to a solution is obtained.

5.3.1 Transistor Selection

The first step in the design of an effective frequency multiplier is selection of a suitable transistor. The FET must have a useful operating bandwidth in excess of 18 GHz and a high drain-gate avalanche voltage, as the minimum gate voltage, $V_{g,min}$, is expected to be quite large to obtain the small conduction angle required for high $5th$ harmonic output content, as described in Section 4.2.2. The second peak in the harmonic drain current versus conduction angle characteristic, shown in Figure 4.9, has a magnitude of only 4% of the peak drain current for the $5th$ harmonic. Therefore, in order to get high enough $5th$ harmonic drain current for appreciable output power, the peak drain current must be quite large, perhaps on the order of 100 mA. Most small signal GaAs FETs are not rated to handle drain currents of this magnitude, nor do they have very high drain-gate avalanche voltage ratings.

Power FETs are designed to withstand the higher drain current and drain-gate voltages encountered in power amplifier and oscillator applications. These devices, therefore, are more suitable than small signal FETs for the design of high harmonic FET multipliers. The NEC NE900000 medium power GaAs MESFET was selected for the multiplier. It has a useful operating bandwidth in excess of 20 GHz, saturated drain current $>$ 100 mA,

and maximum drain-gate voltage > 12 V. A chip device was used instead of available packaged devices, to avoid the parasitic package inductance at the drain which limits the performance as it becomes more difficult to effectively resonate the drain capacitance at 18 GHz. Therefore, wirebonding was required to ground the source and to connect the gate and drain to the input and output microstrip lines.

The NE900000 is designed for power amplifier applications and can typically dissipate 800 mW of power with proper heatsinking. This is more than adequate for the low power Class C multiplier mode of operation chosen for this application. Although the peak drain current is large, the average drain current is substantially less, as a result of the low drain conduction angle. Therefore, the power dissipated in the FET is not very high. The next section discusses the FET biasing considerations to obtain the desired drain conduction angle for high $5th$ harmonic current.

5.3.2 Biasing

The FET gate and drain bias voltages were selected to provide the desired Class C multiplier operating characteristics at a drain conduction angle of approximately 140 degrees, as described in Section 4.2.2. The turn-on voltage, V_t, for the NE900000 is -2.7 V. The "knee" voltage in the I-V characteristic occurs at approximately $V_{ds} = 1$ V, corresponding to a drain current of approximately $I_d = 80$ mA. The saturated drain current, I_{dss}, is about 100 mA at $V_{ds} = 3$ V and $V_{gs} = 0$ V. Therefore, it is desirable to keep the peak gate voltage, $V_{g,max}$, as close to 0 V as possible to maintain high peak drain current for the desired conduction angle, without forcing $V_{g,min}$ low enough to exceed the maximum drain-gate voltage. Operation near the knee voltage is also preferable to achieve the output saturation condition.

The conduction angle, assuming ideal sinusoidal drain current pulses, is [36]

$$\theta_t = 2\cos^{-1}\left(\frac{2V_t - V_{g,max} - V_{g,min}}{V_{g,max} - V_{g,min}}\right). \tag{5.5}$$

From Equation 5.5, a conduction angle of 143 degrees is obtained with $V_{g,max} = -1$ V and $V_{g,min} = -6$ V, which gives a gate bias voltage of $V_{gg} = \frac{V_{g,max}+V_{g,min}}{2} = -3.5$ V. Assuming the drain swings into saturation at the knee voltage, with $V_{d,min} = 1$ V, a drain bias voltage of $V_{dd} = 3$ V provides a maximum drain voltage of $V_{d,max} = 5$ V. This bias point,$V_{dd} = 3$ V and $V_{gg} = -3.5$ V, was chosen as it provides reasonably high peak drain current at $V_{g,max} = -1$ V, with acceptable drain-gate voltage of $V_{d,max} - V_{g,min} = 11$ V. In the next section, this bias point is used with the Series IV nonlinear model of the NE900000, to perform Harmonic Balance analysis with various drain terminations.

5.3.3 Output Circuitry

Output circuitry is designed to provide maximum $5th$ harmonic output power to the load, while rejecting the fundamental frequency component and all other harmonics. To accomplish this task, the output termination effectively resonates the FET drain capacitance at the $5th$ harmonic frequency of 18 GHz, while short circuiting the drain at the fundamental frequency and all other harmonic frequencies. This ensures that only the $5th$ harmonic drain current flows through the load and contributes to the output power. It is also desirable that the real impedance presented to the drain be large enough to cause the drain voltage to vary between $V_{d,max}$ and $V_{d,min}$, for the saturation condition. It soon becomes apparent that this desired load impedance is impractically high in a $5th$ harmonic multiplier, and very difficult to transform from the 50 Ω load. From Equation 4.22, the required load resistance is 625 Ω, assuming the $5th$ harmonic drain current is 4% of the peak drain current of 80 mA and the drain voltage swing is $V_{d,max} - V_{d,min} = 4$ V. Therefore, an initial load resistance of 200 Ω was chosen as a starting point for the load

termination.

It was assumed above that a short circuit drain termination is optimal. Dow and Rosenheck [39] suggest that for a 20-40 GHz doubler, an open circuit drain termination at the fundamental frequency provides higher gain than a short circuit termination while the short circuit termination at the fundamental frequency provides higher output power. Maas [36] concludes that an open circuit fundamental drain termination provides unpredictable and potentially unstable results. With short circuit terminations, no voltage can exist at the drain, except for that of the desired harmonic. The effect of an open circuit drain termination at the fundamental is a large fundamental frequency voltage swing at the drain. This could result in the drain-gate avalanche voltage being exceeded in a multiplier with high reverse gate voltage. Short circuit terminations were used for the realization of this multiplier.

Series IV Harmonic Balance analysis provides a powerful feature for termination of each output harmonic in a load specific to that harmonic frequency. Therefore, it is easy to independently terminate each output harmonic with an ideal load reflection coefficient of any value. This principle was used to terminate the drain of the NE900000 for Harmonic Balance analysis. The drain was terminated in ideal short circuits, with $\Gamma_N = 1\angle 180°$, at all output harmonics including the $5th$, in order to verify the harmonic drain current content and set an appropriate input level for simulation to achieve the desired drain conduction angle. No matching circuitry was initially employed on the FET input, and the input level was increased until the desired peak gate voltage was obtained.

Table 5.1 shows the magnitude of the harmonic drain current components relative to the peak drain current, as determined by Harmonic Balance analysis with 11 harmonics, for $V_{g,max} = -0.6$ V and $I_d = 82$ mA. For comparison, Table 5.1 also shows the ideal harmonic drain current components

Table 5.1 Harmonic Current Content for NE900000 with Ideal Short Circuit Drain Terminations

Harmonic	Frequency (GHz)	Ideal cond. angle	NE900000 all shorts
		$\frac{I_n}{I_{d,max}}$	$\frac{I_n}{I_{d,max}}$
1	3.6	0.43	0.43
2	7.2	0.27	0.25
3	10.8	0.096	0.081
4	14.4	0.010	0.008
5	18.0	0.035	0.031

relative to the peak drain current, as calculated using the ideal cosine pulse train conduction angle in Equation 4.20. The magnitudes of the drain current components for the FET terminated in ideal short circuit terminations are very close to the ideal magnitudes for an optimal conduction angle of around 140 degrees. Therefore, this confirms that the FET has the necessary bandwidth for operation at a $5th$ harmonic frequency of 18 GHz and the bias points and gate input voltage level are suitable to provide the desired drain current conduction characteristics.

Next, the ideal termination at the $5th$ harmonic was adjusted to effectively resonate the drain capacitance, C_{ds}, while providing a real impedance to the drain to maximize the output power at 18 GHz. An approximate solution to the desired $5th$ harmonic drain impedance is an inductive reactance equal to and in parallel with the drain capacitive reactance, in order to resonate C_{ds}. This inductive reactance is in parallel with 200 Ω resistance, which was assumed above to give the maximum drain voltage swing. Assuming C_{ds} = 0.12 pF, the estimated load impedance at the drain is Z_L(18 GHz)= 23.9 + j64.9 Ω, which gives a voltage reflection coefficient of $\Gamma_L = 0.71\angle 71°$.

The Harmonic Balance analysis was run again, with the $5th$ harmonic of the FET drain terminated in $\Gamma_5 = 0.71\angle 71°$, while the other harmonics remained terminated in shorts with $\Gamma_N = 1\angle 180°$. The $5th$ harmonic termination was optimized in the analysis to provide maximum output level at 18 GHz. The maximum output level at 18 GHz was -8.3 dBm, for a $5th$ harmonic termination with voltage reflection coefficient of $\Gamma_5 = 0.56\angle 78°$, which is comparable to the approximate termination, and corresponds to a load of 70.6 Ω inductive reactance in parallel with 113 Ω of resistance.

The next step was to synthesize microstrip circuitry to transform the 50 Ω load impedance to the desired $5th$ harmonic impedance at the FET drain, while providing short circuit terminations at the other harmonic frequencies. Designing a matching circuit to provide the desired $5th$ harmonic impedance is relatively straightforward, but terminating the other harmonics in short circuits is a bit more difficult. This difficulty arises from the fact that distributed microstrip circuitry designed to be a short circuit at the fundamental frequency and odd harmonics is most likely to be an open circuit at the even harmonics. Also, a short circuit at the fundamental frequency is also likely to be a short circuit at the desired $5th$ harmonic, not the required termination impedance. Good short circuit terminations at the fundamental frequency and second harmonic components are of primary importance, as these are the largest harmonic components of the drain current.

The circuitry chosen to achieve this difficult harmonic termination objective was realized as a combination of a coupled line bandpass filter, BPF1, at the $5th$ harmonic frequency, a section of 50 Ω transmission line, TL1, a single stub matching circuit, M2, and the drain choke, RFC3. An additional advantage in using a coupled line filter in the output circuitry is that it provides DC blocking for the drain bias and removes the requirement for a blocking capacitor which is difficult to obtain at 18 GHz. The coupled line bandpass filter is designed as a $2nd$ order Butterworth filter. This filter provides ad-

equate rejection of unwanted harmonics, and a 50 Ω impedance at 18 GHz that can be transformed to the desired $5th$ harmonic drain impedance. The filter is designed using the $2nd$ order Butterworth lowpass filter prototype, with $g_0 = g_3 = 1$ and $g_1 = g_2 = \sqrt{2}$, and three $\lambda/4$ coupled line J-inverter sections [33]

$$Z_o J_1 = Z_o J_3 = \sqrt{\frac{\pi\Delta}{2g_1}}, \tag{5.6}$$

$$Z_o J_2 = \frac{\pi\Delta}{2\sqrt{g_1 g_2}}, \tag{5.7}$$

where Δ is the passband bandwidth as a fraction of the centre frequency and

$$Z_{oe,n} = Z_o[1 + J_n Z_o + (J_n Z_o)^2], \tag{5.8}$$

$$Z_{oo,n} = Z_o[1 - J_n Z_o + (J_n Z_o)^2], \tag{5.9}$$

are the even and odd mode impedances for the nth sections of coupled lines. The even and odd mode impedances were calculated using Equations 5.6 to 5.9 with 5 % bandwidth. The corresponding coupled line circuit dimensions to produce these even and odd mode impedances were estimated using the Series IV LineCalc program, and these coupled lines were used as a starting point for Series IV optimization of the filter. The simulated filter amplitude response and return loss as a function of frequency is shown in Figure 5.13. Figure 5.13 shows the responses as calculated with the Series IV transmission line models, and also the responses as calculated by the Series IV Momentum [43] program, which are labelled 'Momentum' in the figure. The Momentum program uses a numerical electromagnetic technique for simulating planar microwave circuitry, and is useful for comparison purposes and validation of the Series IV transmission line models. From Figure 5.13, it is

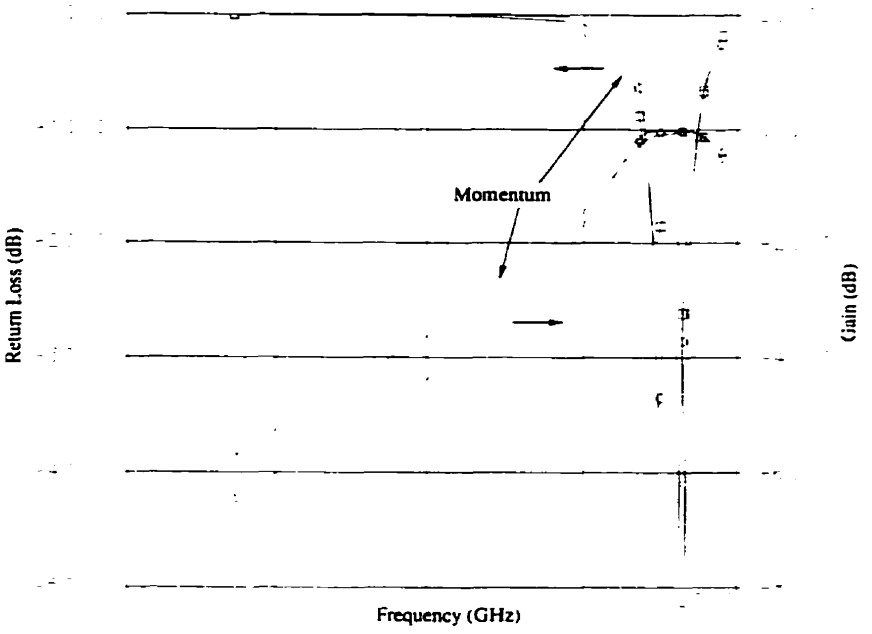


Figure 5.13 Response of the 18 GHz coupled line bandpass filter.

apparent that the bandpass filter has a well matched passband at 18 GHz and substantial rejection at the first and second harmonic frequencies, which have the largest drain current components. The responses using the transmission line models are also very close to those using the electromagnetic simulator, lending confidence to the validity of the Series IV models at 18 GHz.

As $|S_{11}|$ from Figure 5.13 is near 0 dB, the impedance at harmonics other than the $5th$ is essentially reactive and the magnitude of the voltage reflection coefficient is near 1 for a filter providing high rejection. Since $|\Gamma| \approx 1$, a section of 50 Ω transmission line can be used to transform a reactive harmonic impedance to a short circuit at the FET drain, while having little effect on the 50 Ω impedance at 18 GHz. The length of the 50 Ω transmission line, TL1, was varied to obtain an effective drain short circuit at the fundamental frequency.

Table 5.2 Voltage Reflection Coefficient of the Drain Choke and Output Circuitry

Harmonic	Frequency (GHz)	Γ_{choke}	Γ_L
1	3.6	$0.99\angle 0.5°$	$0.99\angle -169°$
2	7.2	$0.97\angle 179°$	$0.96\angle 163°$
3	10.8	$0.99\angle -3.7°$	$0.99\angle 171°$
4	14.4	$0.91\angle 171°$	$0.91\angle 124°$
5	18.0	$0.94\angle 0.1°$	$0.56\angle 78°$

The short circuit at the second harmonic of the fundamental, and at other even harmonics of the fundamental, is provided by the drain choke, RFC3. The choke is similar to the choke described in Section 5.2.3, and consists of a high impedance $\lambda/4$ line at the fundamental frequency of 3.6 GHz. shorted by a combination of a radial stub at 18 GHz and a tuned capacitive short at 3.6 GHz, which includes a 10 pF high Q porcelain microwave chip capacitor. Other higher value porcelain chip capacitors are included in the choke for power supply bypass. The line length is a multiple of $\lambda/4$ at odd harmonics of the fundamental and a multiple of $\lambda/2$ at even harmonics of the fundamental. As a result, the choke appears as an open circuit to the fundamental frequency and odd harmonics and as a short circuit at even harmonics. This behaviour is demonstrated in Table 5.2, which shows the simulated voltage reflection coefficient of the drain choke at various harmonic frequencies.

With the drain shorted at even harmonics of the fundamental by the choke, and at the fundamental frequency by transforming the bandpass filter impedance to the drain, all significant harmonic short circuits are accounted for, except for the $3rd$ and, perhaps, the $7th$. This is not to say that these harmonics will provide appreciable power at the load, as they will be filtered by the bandpass filter. These harmonics will contribute slightly to voltage

Table 5.3 Harmonic Drain Current and Voltage for NE900000 with Output Termination Circuitry

Harmonic	Frequency (GHz)	$\frac{I_n}{I_{d,max}}$	$\lvert V_{ds,n}\rvert(V_{rms})$
1	3.6	0.42	0.10
2	7.2	0.26	0.11
3	10.8	0.076	0.02
4	14.4	0.031	0.04
5	18.0	0.039	0.13

variation at the drain. As these harmonics are relatively small compared to the first and second harmonic components, this voltage variation will be small and not adversely effect the multiplier operation.

The output matching circuit, M2, and the 50 Ω transmission line section, TL1, are optimized to provide a good fundamental frequency short at the drain and a termination voltage reflection coefficient of $\Gamma_5 = 0.56\angle 78°$ at the $5th$ harmonic. After performing this optimization, the voltage reflection coefficients at the harmonics approximate short circuits at harmonics lower than the $5th$ and the desired voltage reflection coefficient of $\Gamma_5 = 0.56\angle 78°$ at the $5th$ harmonic, as shown in Table 5.2. The drain harmonic current components shown in Table 5.3 are comparable to the ideal harmonic components shown in Table 5.1. The corresponding harmonic voltage components at the drain are quite small, as shown in Table 5.3. Table 5.3 indicates that the drain is effectively short circuited at unwanted harmonics by the microwave output circuitry. The next section discusses design of the multiplier input circuitry.

5.3.4 Input Circuitry

As the output drain terminations are being optimized, it is advantageous not to try and maintain a match between the source impedance and the transistor input impedance. The transistor input impedance, and thus the input match condition, is a function of the drain termination characteristics. As these drain termination characteristics change, the input is mismatched which alters the peak gate voltage. This changes the drain conduction angle and the harmonic output content, which makes optimization of the drain characteristics more difficult. Therefore, until a good estimate of the required output circuitry is obtained, a better procedure is to try and maintain a constant peak gate voltage, rather than maintain an input match condition, while the output circuitry is being optimized. After the output circuitry has been optimized, the source impedance can be matched to the input impedance of the harmonically terminated FET drain.

The input circuitry consists of a chip capacitor, an input matching circuit, M1, and a gate choke, RFC2. The capacitor is a 10 pF high Q porcelain microwave chip capacitor which is low impedance at the input frequency of 3.6 GHz and provides DC blocking for the gate bias. The gate choke has very similar characteristics to the drain choke, providing high impedance at the fundamental input frequency and odd harmonics of the input frequency and low impedance at even harmonics of the fundamental frequency. A conjugate match between the source impedance and the gate of the harmonically terminated FET is provided at the fundamental input frequency by the single stub matching circuit, M1.

To estimate the terminated FET input impedance at the fundamental frequency, the large-signal S-parameters of the circuit were extracted with the input level set to provide the desired peak gate voltage. This type of analysis is available in Series IV and allows extraction of full 2-port S-parameters using the Harmonic Balance method under certain bias and power conditions.

These extracted S-parameters can be used in linear analysis. The large-signal input impedance of the harmonically terminated FET was measured in this manner and found to be $Z_{in} = 40.4 - j170.8\ \Omega$. The highly reactive FET input impedance makes wideband matching at the gate very difficult. Fortunately, this effect is mitigated by the effective increase in output bandwidth by a factor of $\times N$ as a result of frequency multiplication, so narrowband gate matching is generally acceptable. Mismatch at the FET gate as a function of frequency causes variation in the output level as a function of frequency, as the drain conduction angle is changing. Another effect caused by poor source matching at the gate is increased sensitivity to changes in source impedance, which would be encountered when the multiplier is driven by the phase shifter, with output impedance as a function of control voltage. This would cause increased residual AM in the combined phase shifter and frequency/phase multiplier.

Single stub tuning, M1, is used to transform the 50 Ω source impedance to the conjugate match impedance of $Z_s = 40.4 + j170.8\ \Omega$. This matching circuit is then optimized to maintain good input match at 3.6 GHz, while simultaneously optimizing the output matching circuitry to maintain high output level at 18 GHz. This operation is similar to the simultaneous conjugate matching condition in amplifier design, except that the input is matched at the fundamental frequency while the output is matched at the $5th$ harmonic frequency. It was determined that an input level of +5 dBm provided the necessary peak gate voltage, when the transistor input impedance is properly matched.

As a final step, the circuit was checked for unconditional stability at the fundamental frequency and all harmonics. This is not entirely necessary for multiplier design, but is practically a good idea. This is because of the difficulty in predicting the harmonic impedance of terminations designed for a specific frequency. This was done by extracting the large-signal S-parameters

as described above, for all significant harmonics of the fundamental frequency, and then performing stability analysis [49]. The necessary and sufficient conditions for unconditional stability, namely that $K > 1$ and $B_1 > 0$ [49], were met at all harmonics of the fundamental input frequency. The next section presents simulation results for the multiplier design.

5.3.5 Simulation Results

The frequency/phase multiplier circuit was simulated, using HP-EEsof Libra Harmonic Balance analysis with 21 harmonics, to assess the performance in providing a substantial output level at 18 GHz, while sufficiently rejecting all undesired harmonic components. An input level of +5 dBm was used for all tests. The drain bias voltage, V_{dd}, was 3 V and the gate bias voltage, V_{gg}, was -3.5 V for all tests.

Figure 5.14 shows the gate and drain voltage waveforms and the drain current waveforms as a function of time, for an input signal frequency of 3.6 GHz. The peak gate voltage of -0.6 V and the corresponding peak drain current of 83 mA, are quite consistent with the expected values obtained by rough calculation. The drain voltage waveform suggests that the drain capacitance is being effectively resonated at the $5th$ harmonic, as the waveform contains an obvious $5th$ harmonic component. Fundamental and second harmonic components of the drain voltage are also not completely eliminated due to the use of nonideal short circuit terminations at these frequencies. These components, however, are not large enough to cause any instability in the FET. The peak to peak drain voltage is smaller than that estimated by rough calculation, but this is not surprising, as a significantly smaller load impedance was used at the drain, due to the difficulties in transforming the large load impedance required for high drain voltage variation at the $5th$ harmonic.

The performance of the multiplier output termination circuitry in remov-

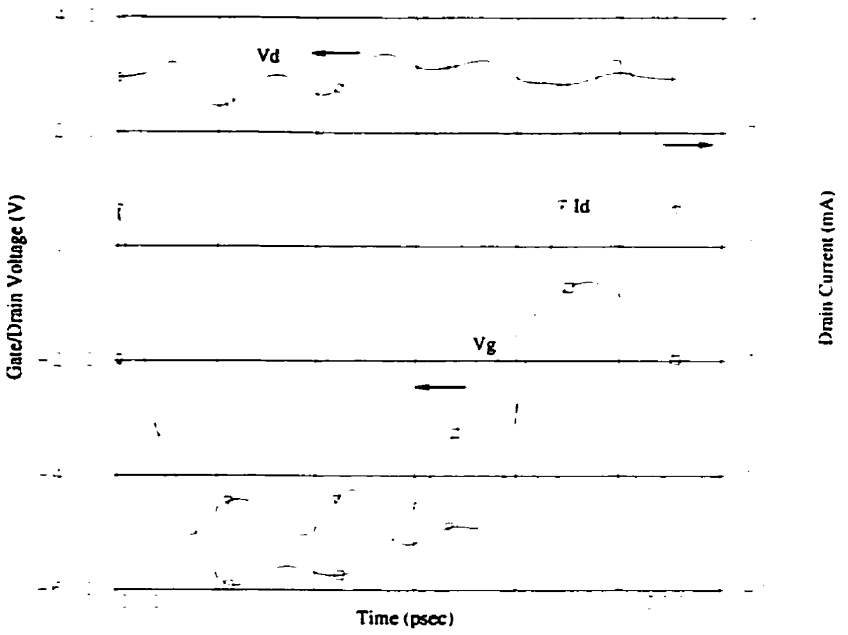


Figure 5.14 Frequency/phase multiplier FET gate voltage, drain voltage, and drain current waveforms.

ing undesired harmonic components is shown in Figure 5.15. Figure 5.15 demonstrates that the output termination circuitry provides very good selectivity of the $5th$ harmonic component at 18 GHz, as the levels of unwanted harmonic components are below 30 dBc.

Figure 5.16 shows the multiplier output level and input return loss as a function of frequency. The frequency scale is relative to the input fundamental frequency sweep. Therefore, the corresponding output frequency span is from 16 to 20 GHz with 1 GHz per division. The multiplier output level exceeds -10 dBm in the passband at 18 GHz, which is a substantial level, and the output bandwidth is on the order of 500 MHz. The input return loss verifies the match at the input fundamental frequency of 3.6 GHz. These simulation results confirm that the FET circuit is operating as a high performance multiplier, with performance that is comparable to that predicted by theory. The next section presents simulation results for the fractional phase shifter combined with the frequency/phase multiplier.

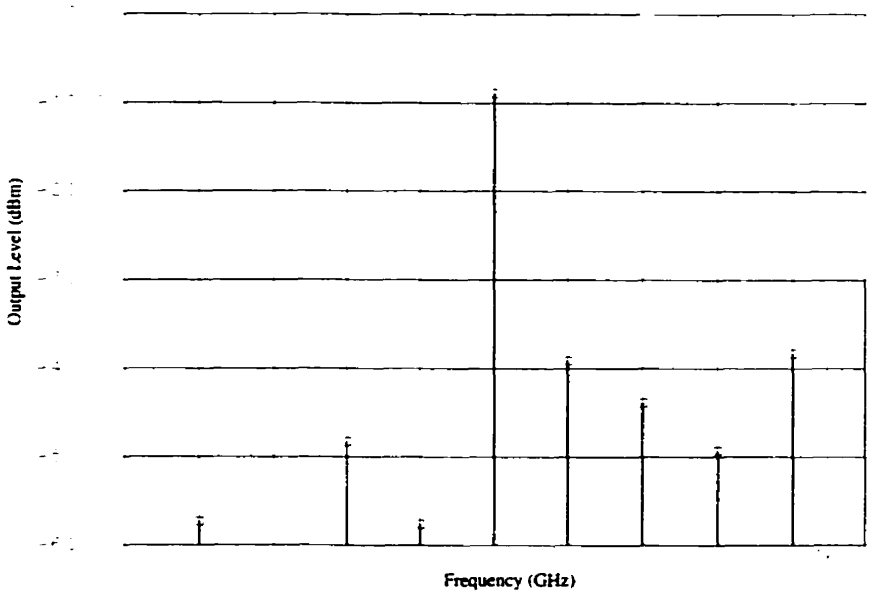


Figure 5.15 Frequency/phase multiplier output signal harmonic content.

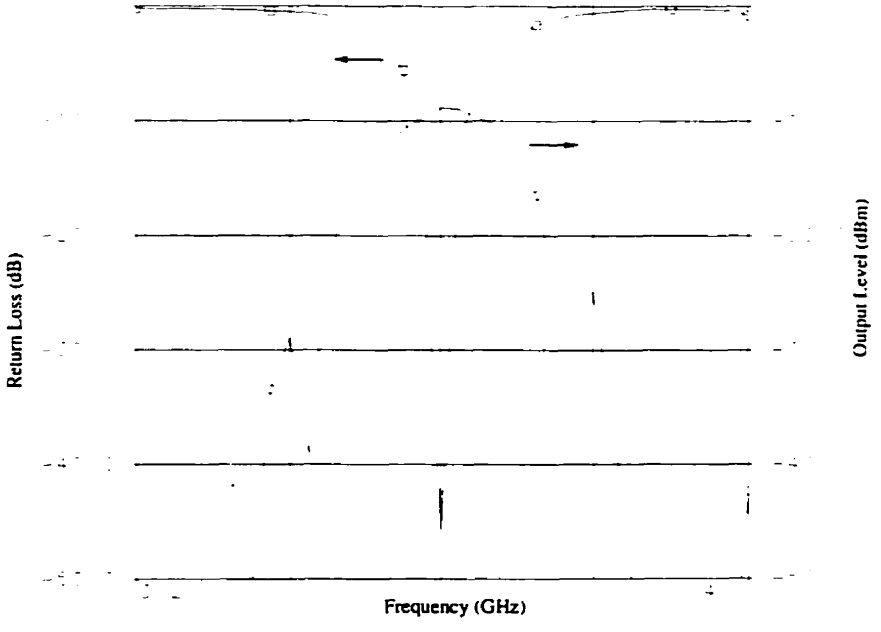


Figure 5.16 Frequency/phase multiplier output level and input return loss as a function of frequency.

5.4 Modulator Simulation

The fractional phase shifter and frequency/phase multiplier circuits were combined to create the full 360 degree phase modulator. This circuit was simulated, using Harmonic Balance analysis with 21 harmonics. The same input level and FET bias voltages used for the multiplier simulation were also used for this simulation. The modulator output signal characteristics at 18 GHz were obtained with a fixed fractional phase shifter phase control voltage. The phase shift performance as a function of the phase control voltage at a fixed output frequency was also obtained.

Figure 5.17 shows the gate and drain voltage waveforms and the drain current waveforms as a function of time for an input signal frequency of 3.6 GHz and control voltage of 0 V. These waveforms are very similar to those presented in Figure 5.14, for the multiplier alone, and suggest that the fractional phase shifter output impedance is properly matched to the terminated FET input impedance to provide the desired drain conduction characteristics. Figure 5.18 demonstrates the modulator output signal harmonic content. These results are also comparable to Figure 5.15 with the multiplier alone.

Figure 5.19 shows the modulator output level and input return loss as a function of frequency, for a control voltage of 0 V. Again, the frequency span is 16 to 20 GHz with 1 GHz per division relative to the output. The output passband characteristics at 18 GHz are comparable to those of the multiplier alone, shown in Figure 5.16. In fact, the output bandwidth is slightly larger and is on the order of 700 MHz. The difference in the two simulation results can be explained by considering that the multiplier was simulated with a wideband 50 Ω source impedance, which is not the output impedance of the phase shifter. Therefore, the phase shifter presents a different input matching characteristic as a function of frequency, which appears to maintain the desired FET conduction characteristics over a wider frequency range.

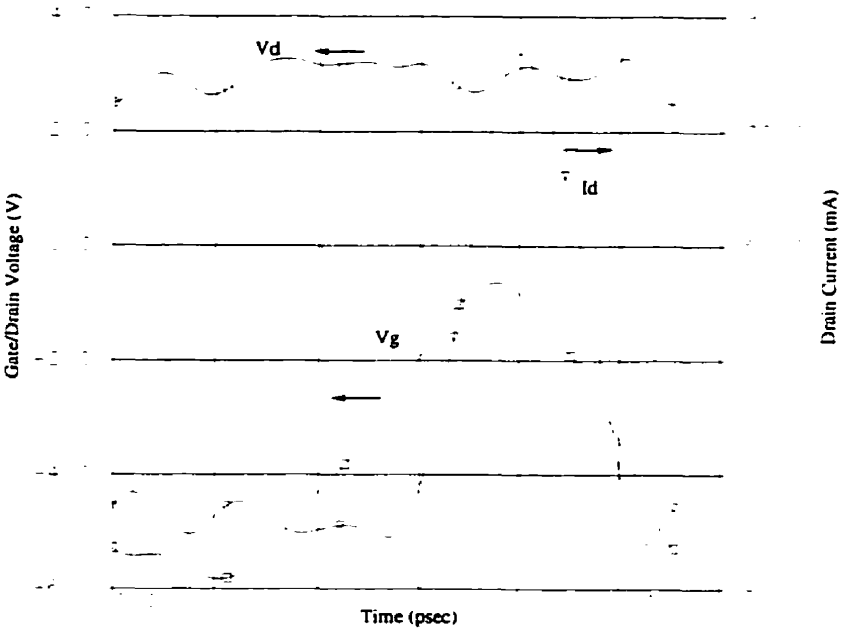


Figure 5.17 Modulator FET gate voltage, drain voltage, and drain current waveforms at a phase shifter bias voltage of 0 V.

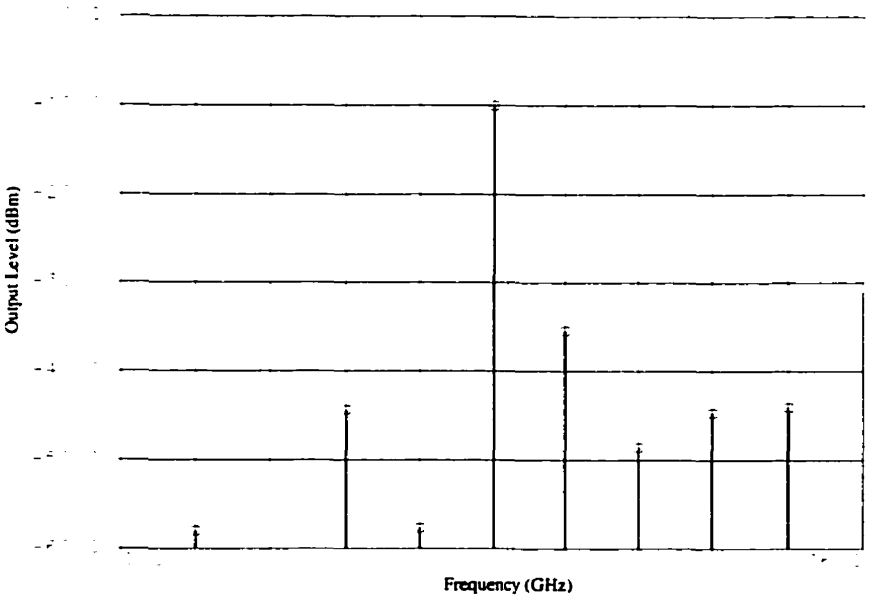


Figure 5.18 Modulator output signal harmonic content at a phase shifter bias voltage of 0 V.

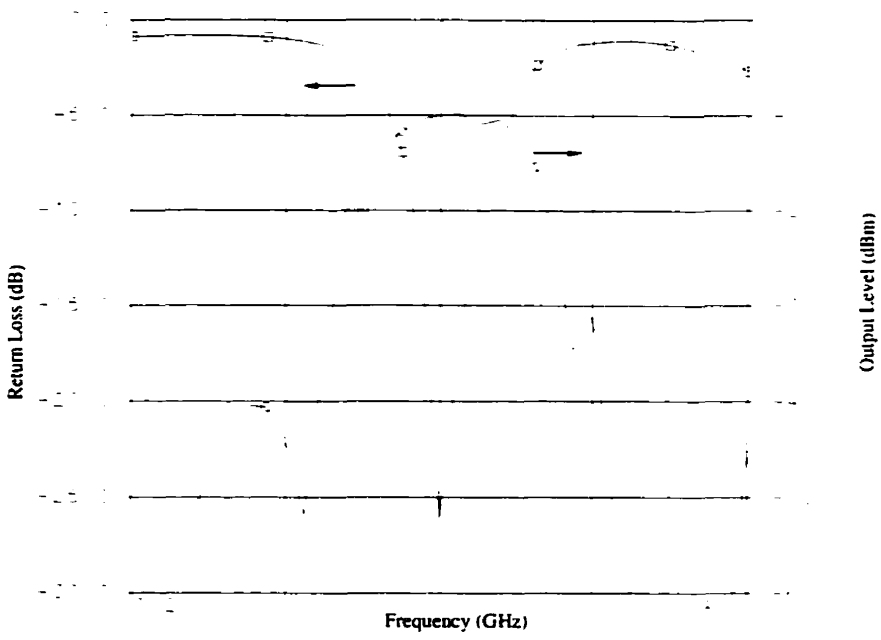


Figure 5.19 Modulator output level and input return loss as a function of frequency at a phase shifter bias voltage of 0 V.

The modulator phase shift and output level at 18 GHz, as a function of bias voltage, is shown in Figure 5.20. The phase shift linearity as a function of bias at 18 GHz is shown in Figure 5.21. From Figure 5.21, the phase error from linear at 18 GHz is 1.5 degrees, over a bias voltage range of 0 to 10 V. From Figure 5.20, this same bias voltage range corresponds to a phase shift of 393 degrees. The phase shift range and linearity are almost exactly $\times 5$ that of the phase shifter alone, shown in Figures 5.10 and 5.11. This gives much confidence in the validity of the proposed method of using a nonlinearity to linearly expand the phase control range. The output level variation over the bias range was on the order of 0.15 dB, and comparable to that of the phase shifter alone, shown in Figure 5.10. This indicates a good FET input match at 3.6 GHz and little additional amplitude variation with control voltage caused by mismatch. The small ripple in the output level is a result of Harmonic Balance error. The amplitude of this ripple is a function

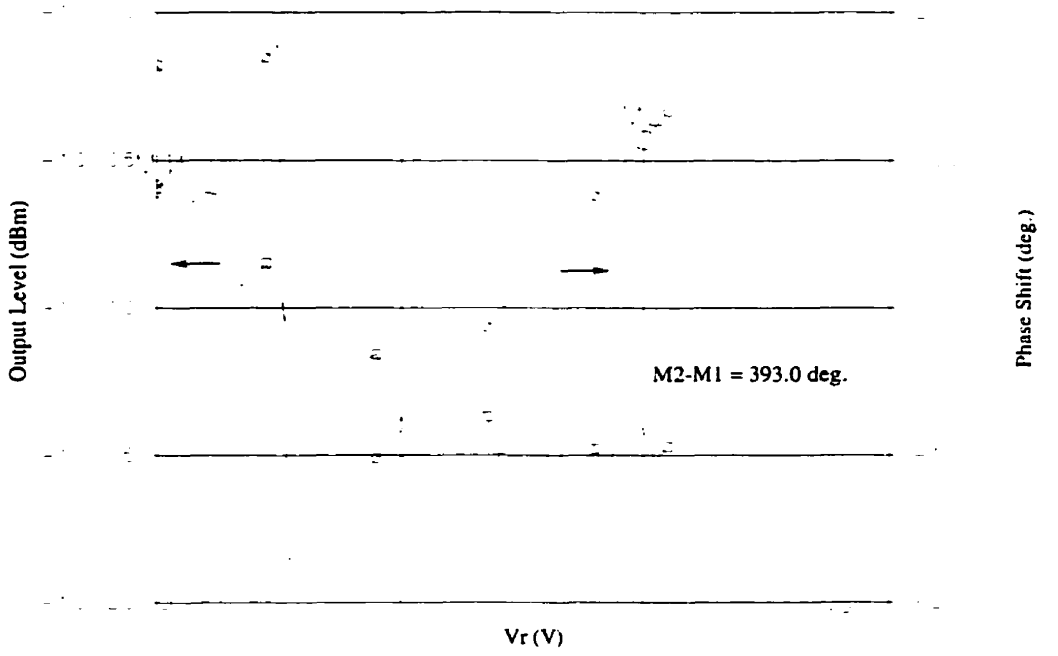


Figure 5.20 Modulator output level and phase as a function of bias voltage at 18 GHz.

of the number of harmonics used in the simulation.

These simulation results suggest a very high performance phase modulator realization with low residual AM, providing linear phase shift of a microwave carrier signal over the full 360 degree range at 18 GHz. The output bandwidth of 700 MHz also suggests that this modulator is appropriate for use with high frequency modulation. These simulation results are encouraging, and validate the design methodology presented in Chapter 4, as well as the tools used to achieve this realization.

5.5 Summary

This chapter presented detailed microwave circuit realizations for the fractional phase shifter and frequency/phase multiplier described theoretically in Chapter 4. The fabrication technology was discussed, along with some of the practical consideration required to realize microstrip circuitry at microwave

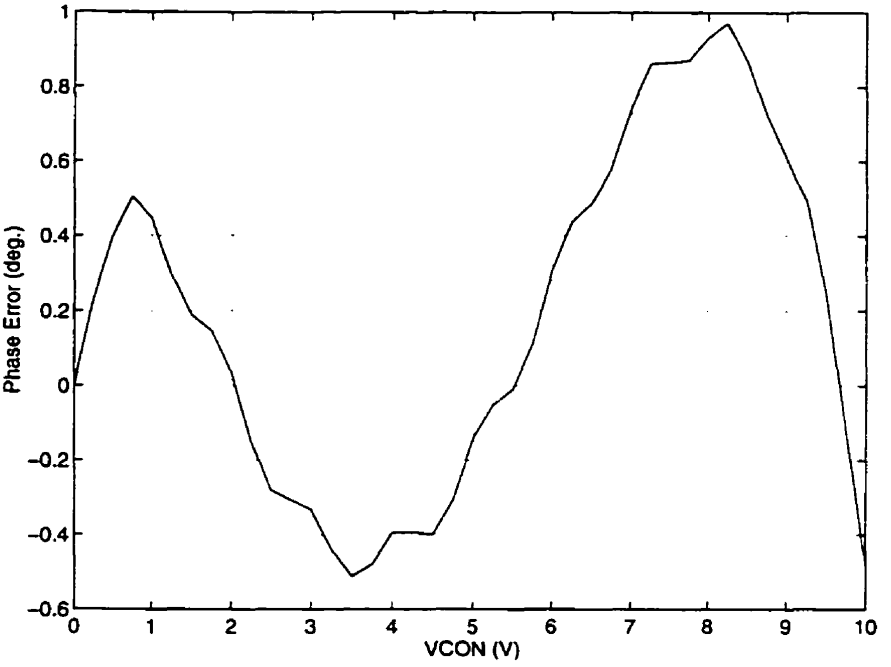


Figure 5.21 Modulator phase linearity as a function of bias voltage at 18 GHz.

frequencies.

The microwave circuitry was designed and simulated using HP-EEsof Libra software. This software performs both linear and nonlinear analysis of microwave circuitry. The fractional phase shifter and frequency/phase multiplier were simulated separately, and then combined together to form the complete phase modulator.

The phase shifter performed very well in providing linear phase shift over a fraction of the required 360 degrees at 3.6 GHz. The phase shifter provided phase control of the carrier over a range of 78.5 degrees, within 0.25 degrees from linear. The multiplier provided an output level of -10 dBm at 18 GHz, over a 500 MHz bandwidth, while maintaining undesired harmonic output levels below -30 dBc.

The two circuits were combined together to form the phase modulator. The circuits performed very well together, and provided effective 18 GHz

carrier phase control over a range of 393 degrees, within 1.5 degrees from linear. The output bandwidth of the combined circuits is on the order of 700 MHz, making this circuitry useful for high frequency modulation.

These simulation results validate the design methodology presented in Chapter 4, and provide much confidence in the method and the tools used to achieve this realization. In Chapter 6, fabrication and test results for this circuit are presented. The circuit was tested for operation as a full range phase shifter at 18 GHz and also as a GMSK modulator at 18 GHz. The simulation results presented in this chapter are compared to the measured results of Chapter 6.

6. DIRECT GMSK MODULATOR RESULTS

In this chapter, details of the prototype modulator fabrication are discussed. Measurement results for the direct GMSK modulator are presented and these results are compared to the simulation results of Chapter 5. Based on the measurements, the effectiveness of the modulator in realizing direct high speed GMSK modulation at 18 GHz is assessed. Recommendations for improvements to the modulator design are suggested.

6.1 Implementation

The fractional phase shifter and frequency/phase multiplier prototype circuits were fabricated using thin film MIC technology, as described in Section 5.1. The fabricated circuits, realized using gold microstrip lines on alumina, are shown in Figures 6.1 and 6.2. The components are attached to the microstrip lines using conductive epoxy. The coaxial to microstrip transitions are short pieces of gold ribbon. All via holes are laser drilled and metalized. Details on the circuit enclosures and transistor mounting are discussed below.

6.1.1 Circuit Enclosures

The microstrip circuits were mounted in metal enclosures for testing. The prototype test jigs for the fractional phase shifter and frequency/phase multiplier are shown in Figures 6.3 and 6.4. All coaxial connectors are high quality SMA type, suitable for use at 18 GHz. Bias voltages for the multiplier are provides via 1000 pF feedthrough capacitors.

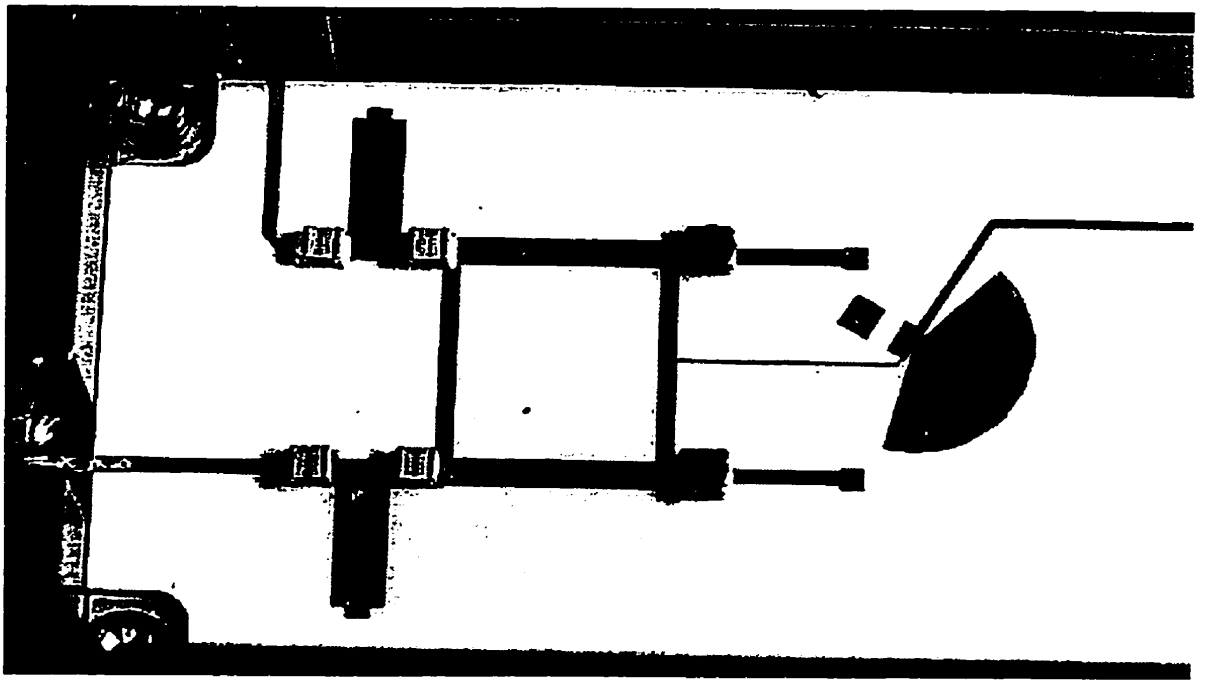


Figure 6.1 Fractional phase shifter prototype microstrip circuit on alumina.

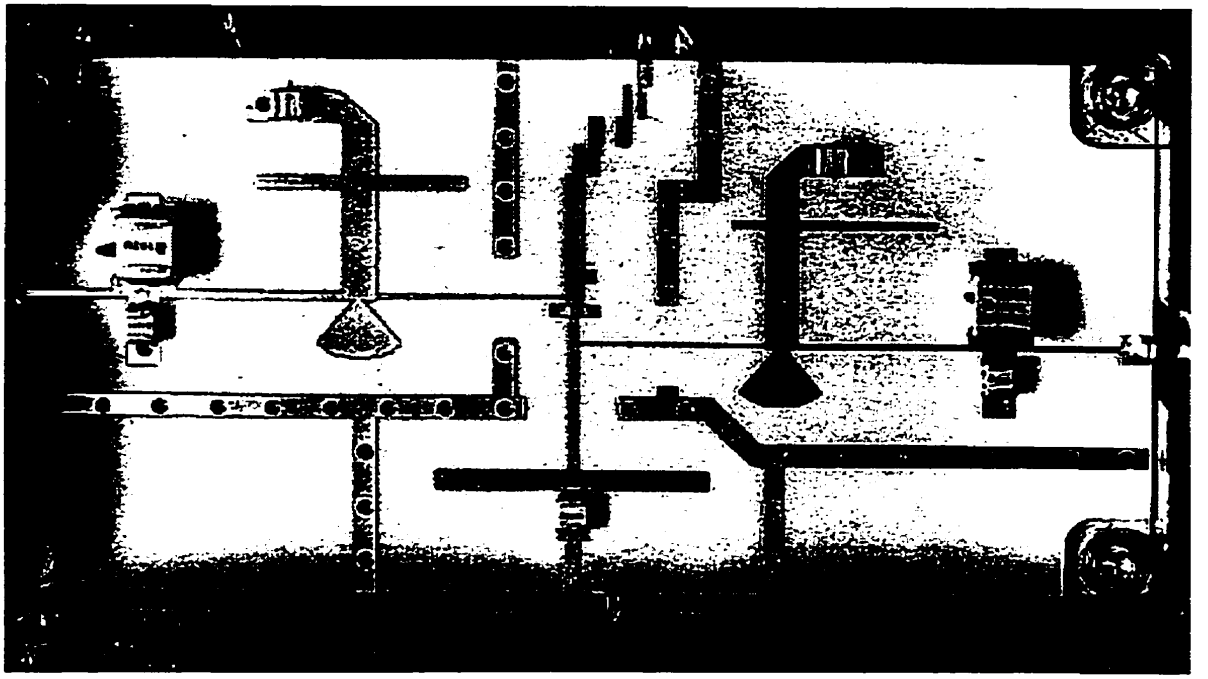


Figure 6.2 Frequency/phase multiplier prototype microstrip circuit on alumina.

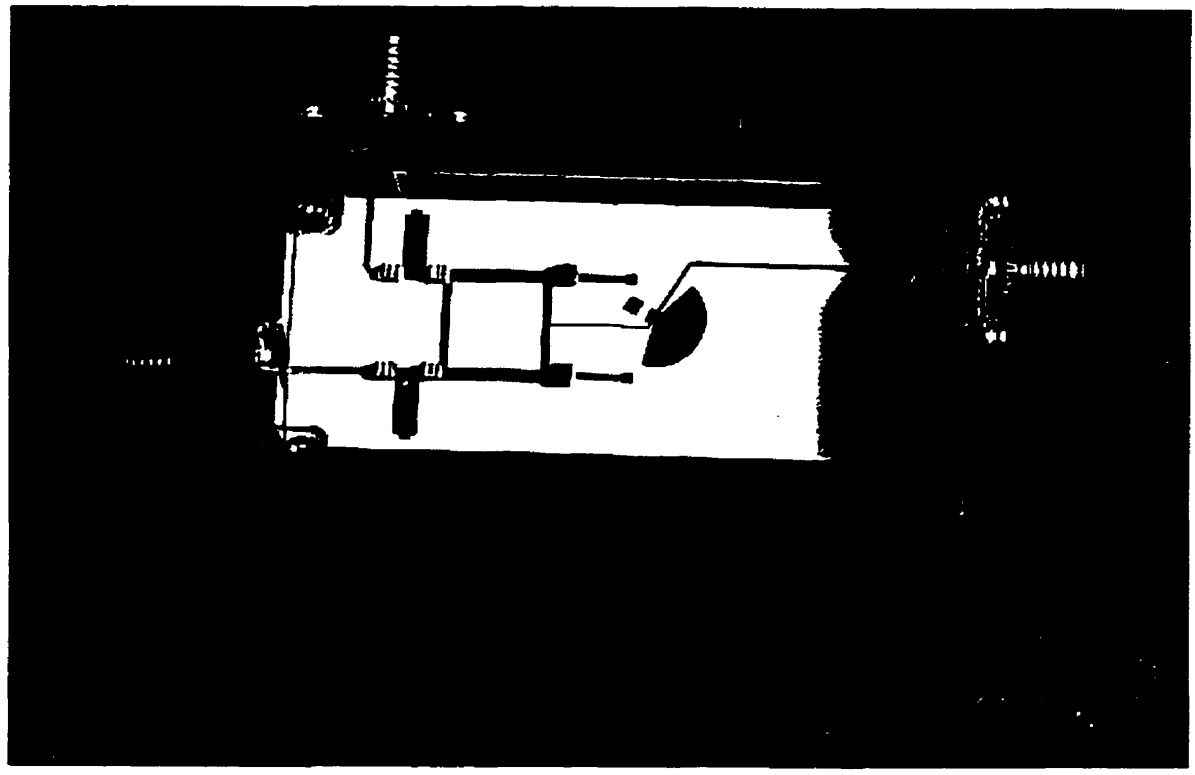


Figure 6.3 Fractional phase shifter prototype test jig.

Metal lids on the enclosures are important, to shield the circuits from external electromagnetic interference (EMI) and also provide consistent circuit behaviour. If the lid is too close to the substrate, however, significant electric field coupling occurs resulting in a change in the effective substrate permittivity, ϵ_{eff}. As long as the height of the lid is at least $10\times$ the substrate thickness, the effect on ϵ_{eff} is negligible [44].

Another concern when enclosing a microwave circuit is package resonances. From a microwave circuit perspective, the metal box functions like a short circuited rectangular waveguide resonator [44]. The frequency of the lowest order resonant mode in rectangular waveguide is typically determined by the largest two dimensions of the box [33]. Thus, the lid cannot be made arbitrarily high, or package resonances may be a problem. Therefore, the dimensions of the enclosure must be small enough to ensure that the cut-off frequency of the lowest order resonant mode is above the oper-

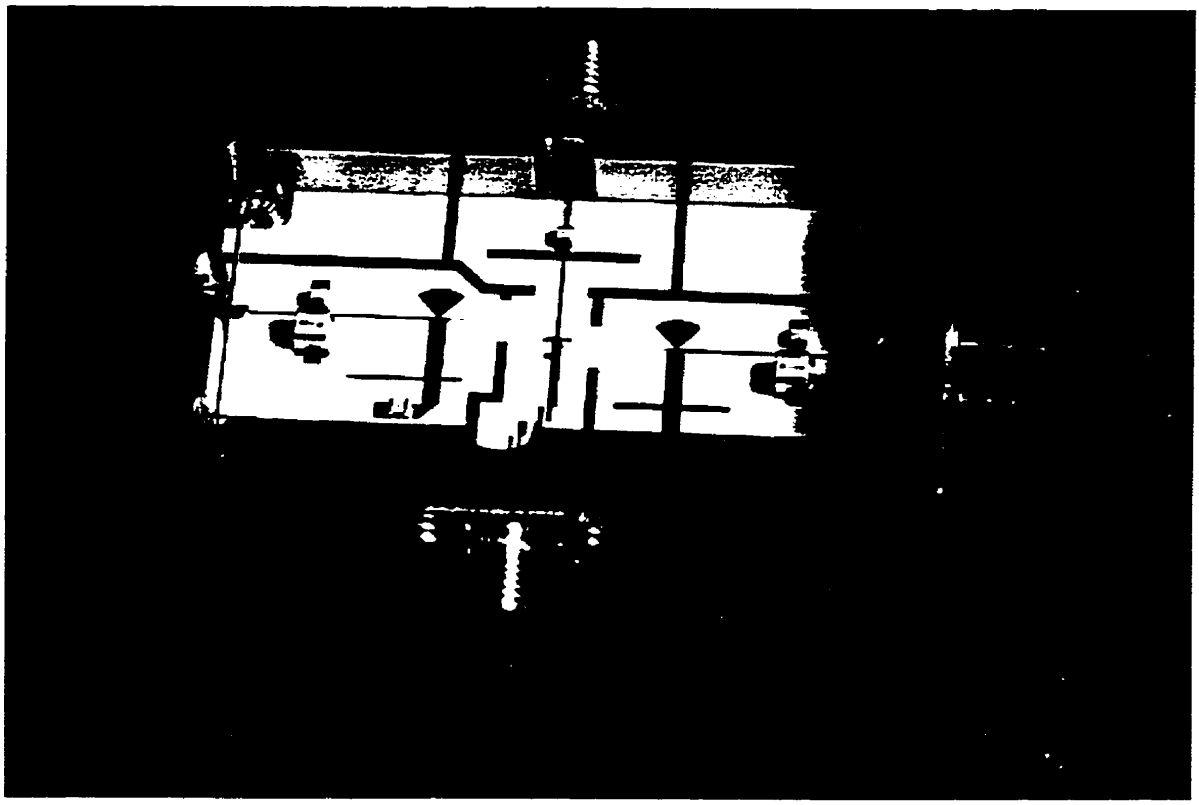


Figure 6.4 Frequency/phase multiplier prototype test jig.

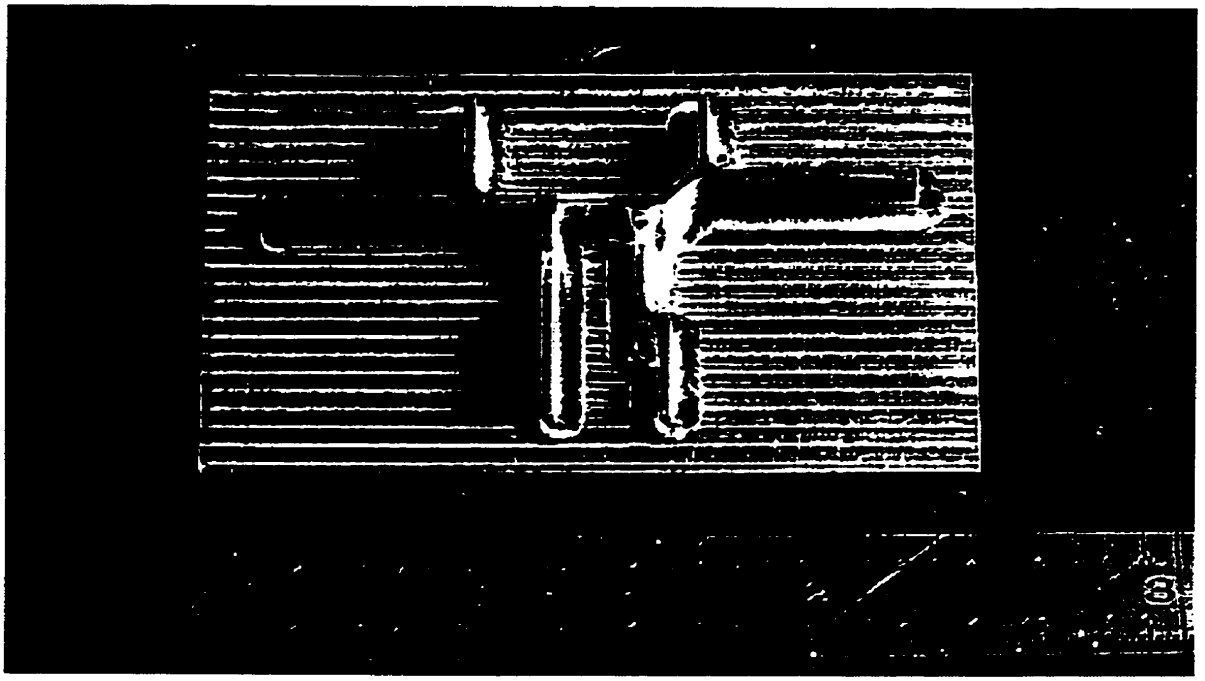


Figure 6.5 Lid for the frequency/phase multiplier test jig enclosure.

ating frequency of the circuit. This is normally not a problem, provided that the overall dimensions of the circuit are not significantly larger than the operating wavelength.

For more complicated circuits, package resonance becomes a concern if the entire circuit is housed in a single enclosure. In this situation, the housing is usually compartmentalized into smaller enclosures. This practice has the added benefit of shielding different parts of the circuit which may be susceptible to pickup of radiated signals. The large dimensions of the input matching circuit and the chokes, relative to the dimensions of the 18 GHz output circuitry, suggested that the multiplier might be susceptible to package resonances. Also, FET oscillation might be possible as a result of radiation and feedback coupling of one of the many harmonics present in the circuit. For these reasons, the multiplier enclosure was separated into smaller compartments. The lid to the enclosure was milled out to provide the sidewalls of the smaller enclosures, as shown in Figure 6.5. The milled

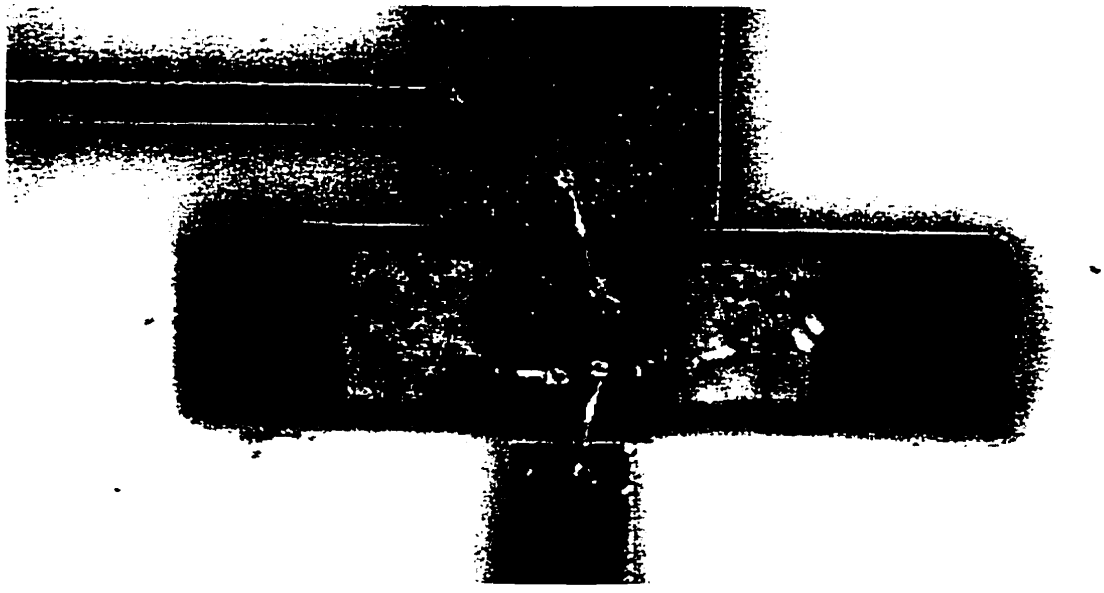


Figure 6.6 Frequency/phase multiplier MESFET mounting and wirebonding.

out sidewalls rest on grounded microstrip traces, shown in Figure 6.2 which serves to enclose the different sections of the circuit.

6.1.2 Transistor Mounting

The NE900000 chip FET was mounted in contact with the metal enclosure, to provide good heat sinking. Although the FET is not dissipating much power in this application, this is the safest mounting procedure, as alumina is not a very good conductor of heat. The FET mounting is shown in Figure 6.6. A 20 mil. high metal pedestal is inserted in a 20 mil. by 85 mil. laser drilled slot in the alumina, and attached to the metal substrate carrier. The chip FET is bonded to the top of the pedestal, the height of which is chosen to make the top of the FET level with the surface of the substrate. Connections to the FET gate (bottom of Figure 6.6), drain (top of Figure 6.6), and source (two wires) are made using 1 mil. diameter gold wires. The next section describes the philosophy used in testing the prototype circuits.

6.2 Testing Philosophy

The modulator was tested for various performance parameters using three main test setups. These test setups are described in detail below. Where feasible, testing was designed so that the measured results would be directly comparable to the simulation results presented in Chapter 5. Some of the results presented in the simulations are impractical to make using microwave measurement instruments and techniques, and thus, were not measured. What is presented is a comprehensive set of measurements for evaluating the performance of the circuitry in realizing direct GMSK modulation at microwave frequency, which was one of the main objectives of this research.

The modulator was deliberately fabricated as two separate circuits, the fractional phase shifter portion and the frequency/phase multiplier portion. This enabled evaluation of the performance of both circuits individually, and the performance of the circuits together as a complete modulator.

Optimal baseband circuitry for generation of the modulating signals was not designed specifically for this application. For evaluation purposes, commercially available test equipment was used to generate representative baseband modulation signals.

6.3 Fractional Phase Shifter Performance

The performance of the fractional phase shifter was measured separately before being combined with the frequency/phase multiplier using the test setup described below. In order for the complete modulator to perform as proposed, the phase shifter must provide linear control of the carrier signal phase as a function of bias voltage, over a minimum range of $360/5 = 72$ degrees. It is also desirable that there be low carrier amplitude variation as the bias signal is varied, to preserve the constant envelope property of the modulated signal.

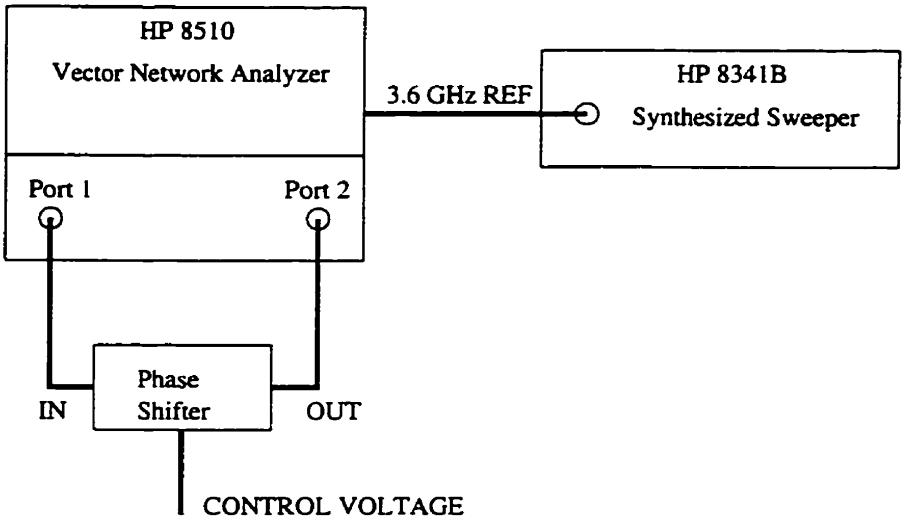


Figure 6.7 Test setup for measuring the fractional phase shifter performance parameters.

6.3.1 Test Setup

The fractional phase shifter performance was determined using the test setup shown in Figure 6.7. The HP8510 vector network analyzer was used with the HP8341B synthesized sweeper to provide full 2-port S-parameter measurements of the phase shifter as the DC bias voltage on the reverse biased termination varactors was varied. At each DC bias point, the 2-port S-parameter measurements as a function of frequency were stored in separate data files via GPIB control of the HP8510. From these data files, the S-parameters for the phase shifter are plotted as a function of frequency at specific bias voltages, or as a function of bias voltage at specific frequencies.

6.3.2 Measurement Results

The fractional phase shifter amplitude response ($|S_{21}|$) and phase linearity (flattened $\arg(S_{21})$) as a function of frequency are shown in Figures 6.8 and 6.9 for various bias voltages. The return loss ($|S_{11}|$) as a function of frequency is shown in Figure 6.10 for various bias voltages. The shape of Figures 6.8

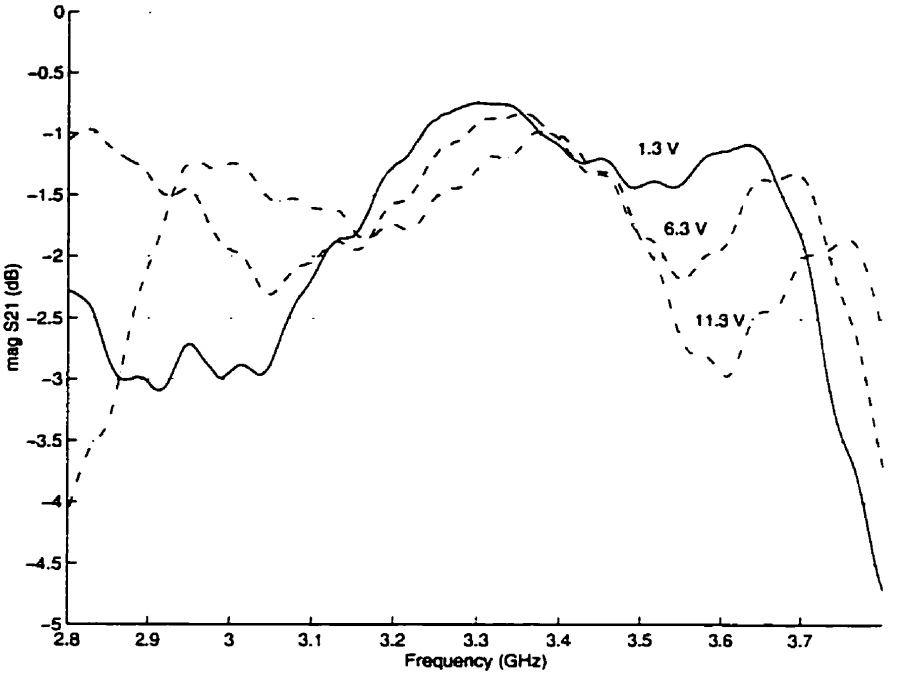


Figure 6.8 Fractional phase shifter amplitude response as a function of frequency for several bias voltages.

and 6.9 is consistent with the simulated response results shown in Figures 5.7 and 5.9. The centre of the responses, however, is slightly lower in frequency. The return loss shown in Figure 6.10 is also comparable to the simulation results of Figure 5.8, although split into two distinct minima. The difference between these measured results and the simulations arises from slight variations in a number of circuit parameters. The coaxial to microstrip transitions, for example, used in the prototype implementation were not included in the simulations. These transitions are slightly inductive and cause variation in input return loss. This increased return loss ripple also manifests itself as increased amplitude response ripple. Small variations in the substrate relative permittivity as well as variations in reactive termination characteristics such as varactor parasitic package capacitance and varactor doping profile also cause slight variations in the phase shifter passband characteristics.

The low loss through the phase shifter (0.5 to 1.5 dB at 1.3 V) is also

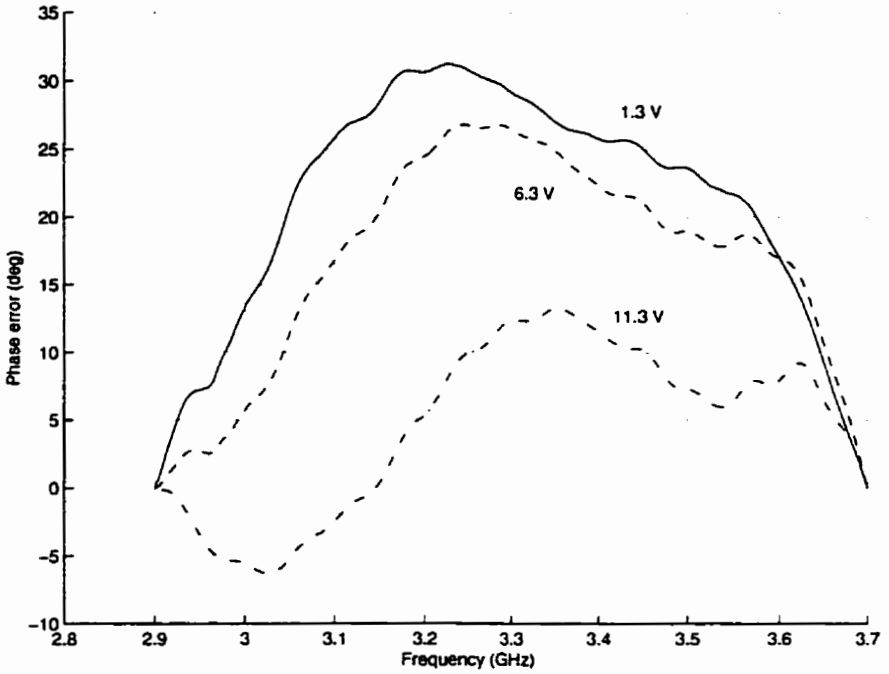


Figure 6.9 Fractional phase shifter phase distortion as a function of frequency for several bias voltages.

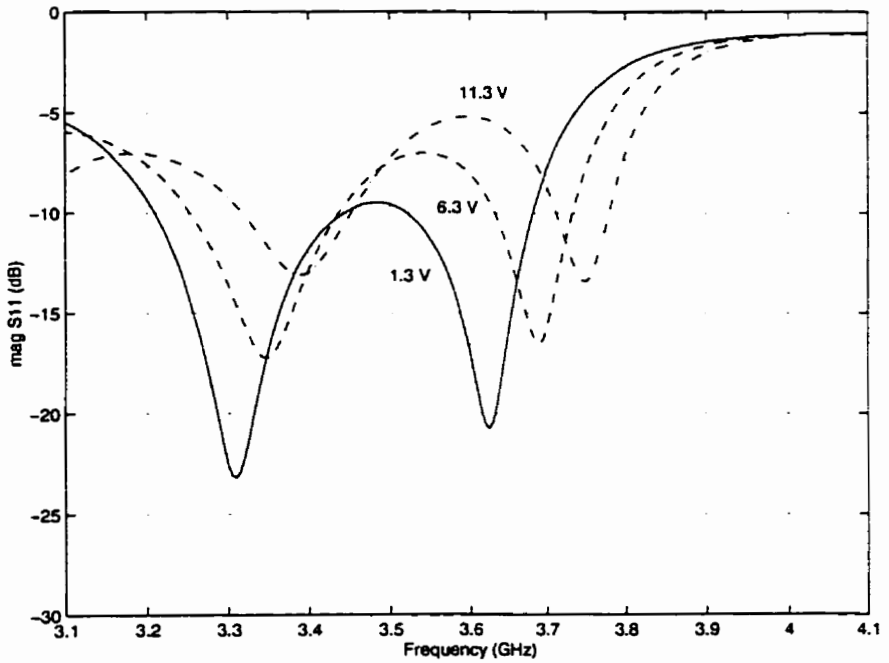


Figure 6.10 Fractional phase shifter return loss as a function of frequency for several bias voltages.

comparable to simulation, which implies good reactive reflective terminations, with low loss and high Q. From these results, it is apparent that the phase shifter is operating properly as a reflective microwave device.

As a result of the slight variations in circuit parameters, one would expect the optimal phase shift linearity as a function of bias to occur at a slightly different frequency than 3.6 GHz, which was the frequency optimized for in the simulations. This assumption is supported by Figure 6.12, which shows the phase shift linearity of the fractional phase shifter as a function of bias voltage at an operating frequency of 3.26 GHz. The phase error from linear at 3.26 GHz is on the order of 0.3 degrees, over a bias voltage range of 0 to 12.5 V, corresponding to a phase shift of 72.2 degrees. The measured phase shift linearity at 3.26 GHz is comparable to the optimum phase shift linearity obtained by simulation at 3.6 GHz. The reduction in optimal performance frequency can be attributed to a reduction in the varactor doping profile constant, γ, an increase in parasitic varactor package capacitance, C_p, an increase in the varactor maximum capacitance, C_o, or a combination of all three. The phase shift range as a function of bias voltage at 3.26 GHz is shown in Figure 6.11. The range at 3.26 GHz is also comparable to the simulation range at 3.6 GHz. The measured range at 3.6 GHz was reduced, which indicates an increase in C_p and the flattening effect described in Section 4.1.2. Another difference in the measured and simulated results is that more change in bias voltage is required to obtain a comparable phase shift range to simulation. This also supports the assumption of slightly reduced varactor γ and/or increased C_o values.

The measured residual amplitude modulation as a function of bias was slightly higher than predicted by simulation. The amplitude variation over the operating bias voltage range of 0 to 12.5 V at 3.26 GHz was 0.8 dB as shown in Figure 6.13. Although still reasonably small, this amplitude variation is significantly higher than predicted by the simulation results of

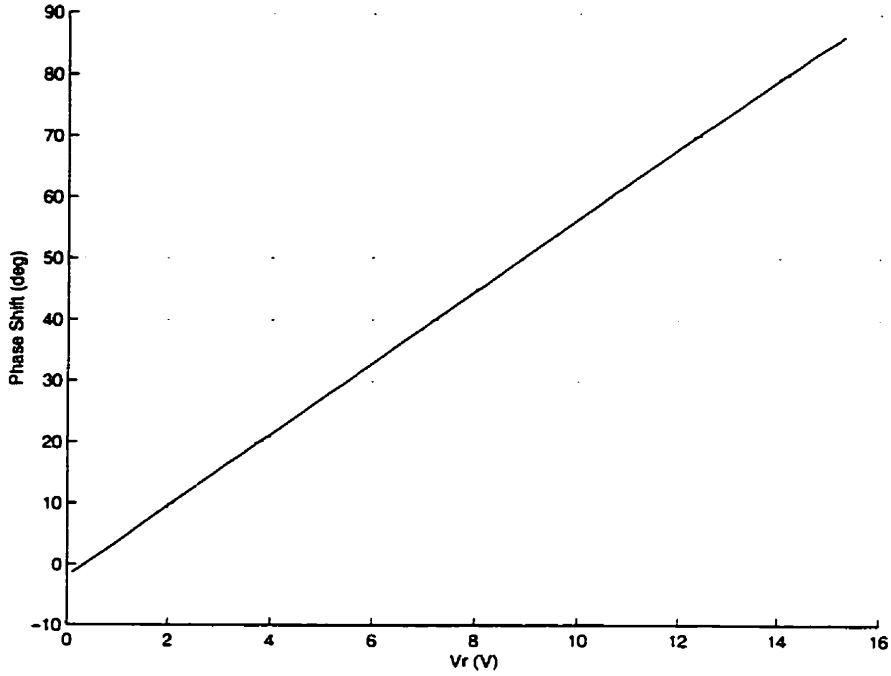


Figure 6.11 Fractional phase shifter phase shift as a function of bias voltage at 3.26 GHz.

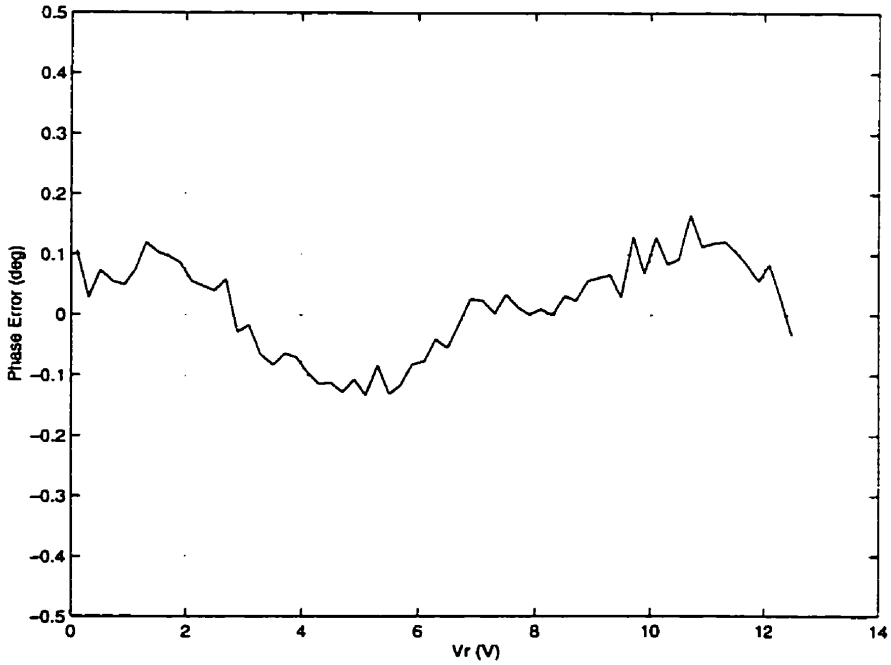


Figure 6.12 Fractional phase shifter phase shift linearity as a function of bias voltage at 3.26 GHz.

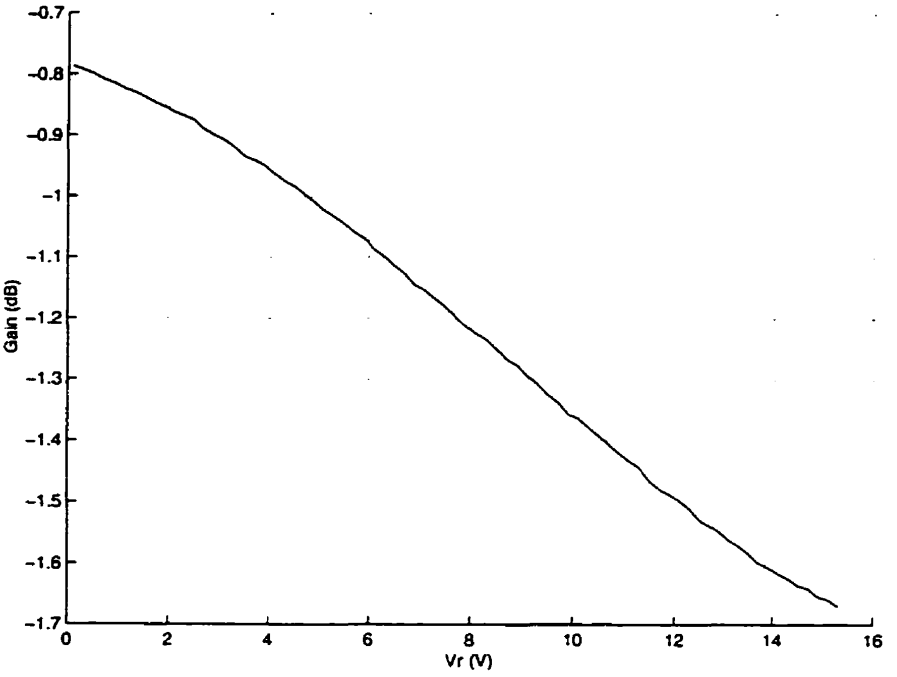


Figure 6.13 Fractional phase shifter amplitude variation as a function of bias voltage at 3.26 GHz.

Section 5.2.5. This indicates that the parasitic varactor resistance varies somewhat with bias. This parameter was assumed constant for the simulations. The return loss variation, and amplitude response ripple, is also more sensitive to variations in the varactor termination resistance due to the mismatch at the input and output microstrip transitions.

Figures 6.11 and 6.12 demonstrate the excellent range and linearity performance of the fractional range phase shifter. Although slightly off frequency, these results are very encouraging and lend confidence to the realization process and the simulation tools and models that have been used. No attempt was made with this implementation to tune the phase shifter for optimal performance at the simulation frequency. It was determined that the phase shifter was performing well enough to prove the feasibility of GMSK modulation in the manner proposed in the research objectives. Therefore, a slightly lower operating frequency was chosen for further testing with the

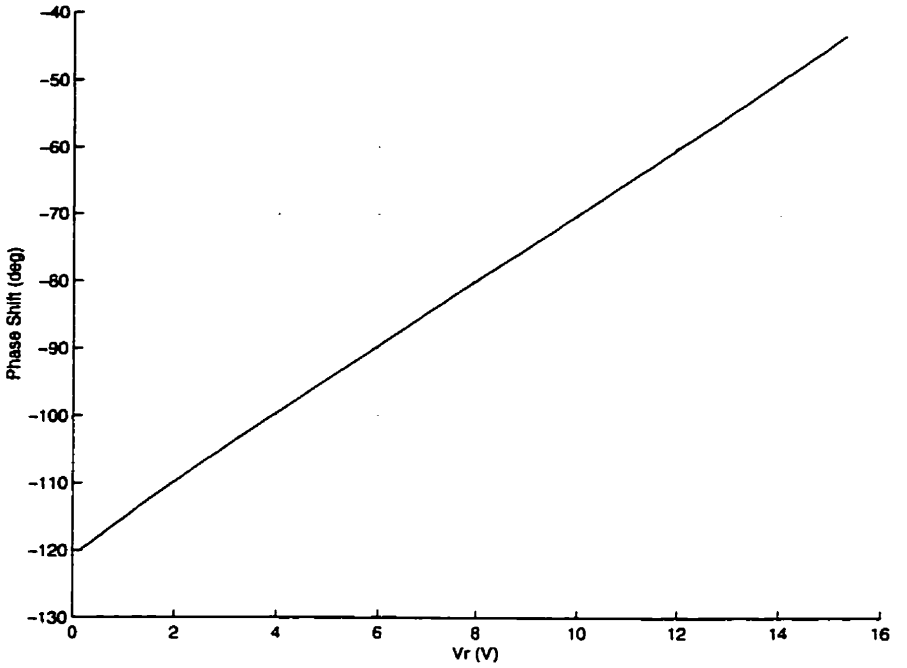


Figure 6.14 Fractional phase shifter phase shift as a function of bias voltage at 3.53 GHz.

complete modulator. The chosen operating frequency of 3.53 GHz is high enough to be within the passband of the frequency/phase multiplier, but still has reasonably low phase distortion as a function of bias voltage. Figures 6.14, 6.15, and 6.16 demonstrate a phase shift range of 72.6 degrees from 0.9 to 15.3 V, within 0.6 degrees from linear, with residual amplitude modulation of 0.8 dB. The next section presents measurement results for the frequency/phase multiplier.

6.4 Frequency/Phase Multiplier Performance

The performance of the frequency/phase multiplier was also measured separately using the test setup described below, before being combined with the fractional phase shifter. In order for the complete modulator to perform as proposed, the multiplier must provide an output signal at $\times 5$ the input signal frequency with appreciable output level. It also must provide sufficient selectivity at the output to reject the fundamental frequency component and

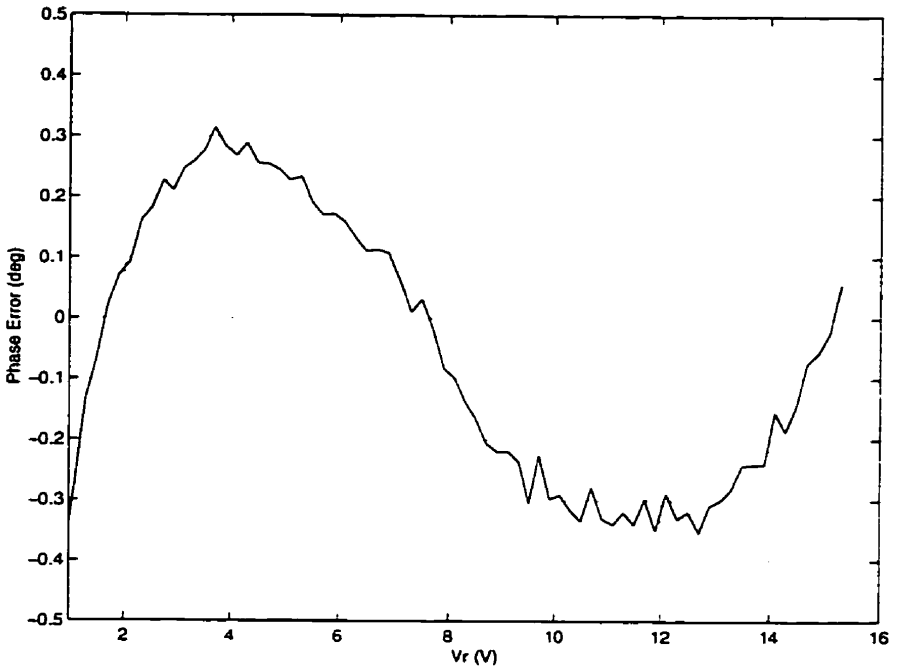


Figure 6.15 Fractional phase shifter phase shift linearity as a function of bias voltage at 3.53 GHz.

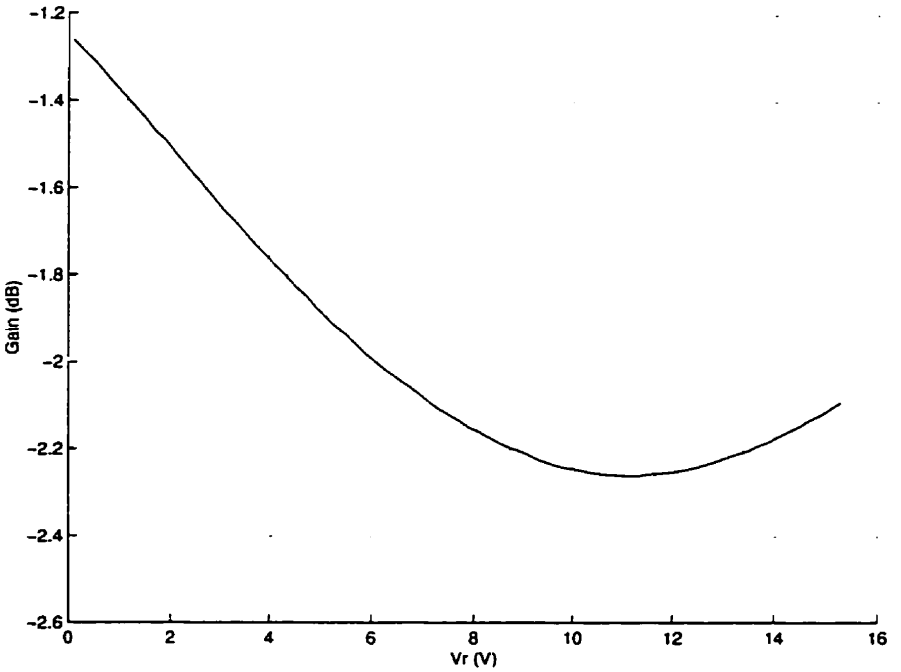


Figure 6.16 Fractional phase shifter amplitude variation as a function of bias voltage at 3.53 GHz.

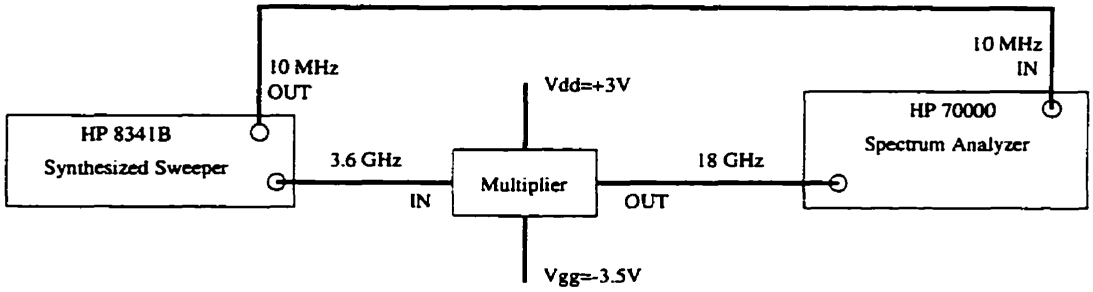


Figure 6.17 Test setup for measuring the frequency/phase multiplier performance parameters.

all undesired harmonic components of the fundamental. In addition, it is desirable that the multiplier perform as a hard-limiter, providing an output signal with constant amplitude envelope and removing slight variations in input signal amplitude.

6.4.1 Test Setup

The frequency/phase multiplier performance was investigated using the test setup shown in Figure 6.17. The HP8341B synthesized generator was used to provide a stable CW input signal in the range of 3.6 GHz. The frequency multiplied output signal spectrum was observed using an HP70000 spectrum analyzer. The multiplier gate and drain bias voltages were set as in the simulations to -3.5 V and +3 V, respectively, for all measurements.

6.4.2 Measurement Results

The multiplier output level as a function of frequency around 18 GHz was measured by slowly sweeping the HP8341B output frequency around 3.6 GHz, with the HP70000 spectrum analyzer trace set in 'hold' mode to store the trace as the HP8341B frequency was swept. The multiplier output level as a function of frequency is shown in Figure 6.18, for an input level of +5 dBm. The output frequency span of 17.8 $\pm$ 1 GHz corresponds to an input

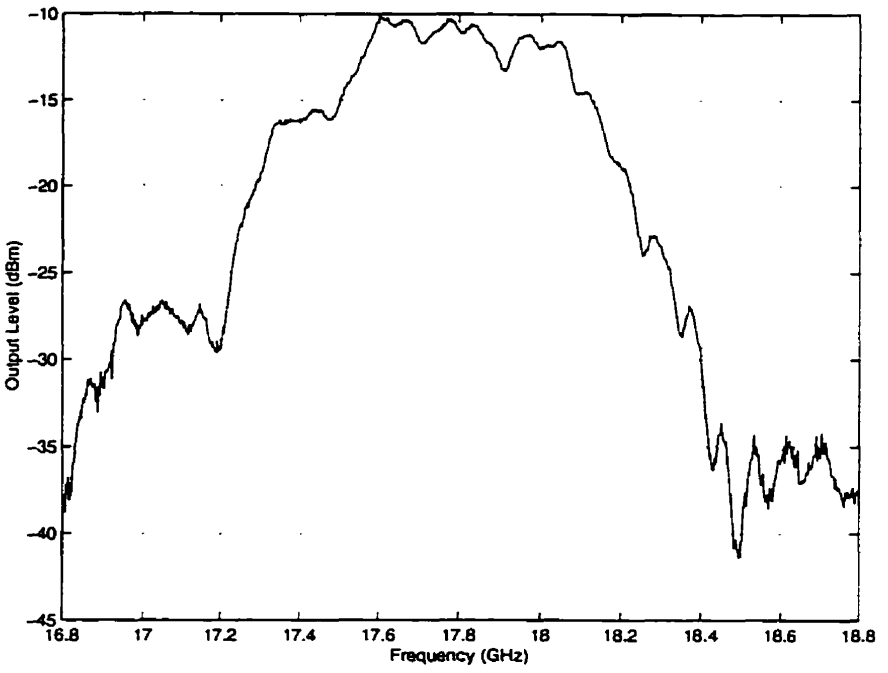


Figure 6.18 Frequency/phase multiplier output level as a function of frequency.

frequency sweep of 3.56 ± 0.2 GHz.

Figure 6.18 demonstrates that the multiplier performance is comparable to that predicted by the simulations of Section 5.3.5. The output level approaches -10 dBm in the passband, which is a reasonable output level at 18 GHz and comparable to the simulations. The output passband bandwidth is on the order of 500 MHz, which is also comparable to the simulations and suggests that the multiplier is useful for high data rate modulation. Like the phase shifter, the passband seems to be shifted slightly lower in frequency and has a bit more amplitude ripple than the simulations. Both of these observations may be attributed to a combination of slightly different substrate relative permittivity and coaxial to microstrip transition mismatch, which was not accounted for in the simulation.

The multiplier output selectivity in extracting the 5th harmonic of the input signal was also verified. Table 6.1 lists the measured multiplier output

Table 6.1 Frequency/phase Multiplier Output Harmonic Levels

Harmonic	Frequency (GHz)	Output Level (dBm)	Output Level (dBc)
1	3.52	-51	-41
2	7.04	-52	-42
3	10.56	-47	-37
4	14.08	-55	-45
5	17.60	-10	—
6	21.12	-44	-34

harmonic levels for a 3.52 GHz CW input signal at +5 dBm. The undesired harmonic levels are all < -30 dBc. and comparable to those predicted by the simulations. The undesired harmonic levels also vary somewhat as the input frequency is varied, but are all comparable to the levels shown in Table 6.1. These results indicate that the multiplier FET drain circuit is functioning properly and providing adequate rejection of all undesired harmonic components.

The multiplier performance as a hard-limiter was also measured, by varying the input level around +5 dBm. The multiplier output level as a function of frequency for input levels of +4. +5, and +6 dBm is shown in Figure 6.19. As discussed in Section 4.2.2, the hard-limiting performance of the multiplier was not expected to be very good, due to the difficulties in obtaining an output saturation condition in a high harmonic multiplier. This suspicion is confirmed by Figure 6.19, which shows significant output level variation with varying input level.

The output level variation with input level is a function of frequency, as a result of variation in the gate conduction angle as described in Section 5.3.4. Figure 6.20 shows the output level variation as a function of input level

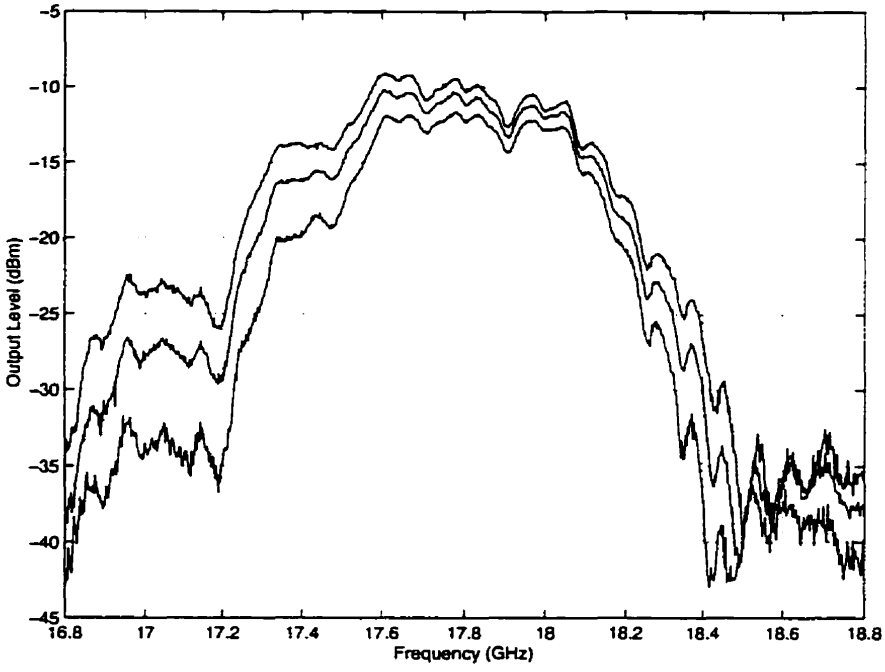


Figure 6.19 Frequency/phase multiplier output level as a function of frequency for input levels of +4, +5, and +6 dBm.

for several frequencies. The best hard-limiting performance is at 18 GHz, where there is a slight reduction in level variation from input to output. At other frequencies, there is nearly linear operation, or slightly increased level variation. This means that although the multiplier is not removing input level variation significantly, it is also not contributing significantly to output level variation.

The frequency/phase multiplier measurement results provide a high degree of confidence in the methods and models used for upper microwave frequency simulation. Of particular concern was the accuracy of the GaAs FET nonlinear model as well as the microstrip transmission line model at 18 GHz. Judging from the agreement between the simulation and measurement results, these models could be considered to accurately predict the behaviour of circuits designed at these frequencies, and are reliable tools in the design of future circuits. This lends confidence in the extension of these

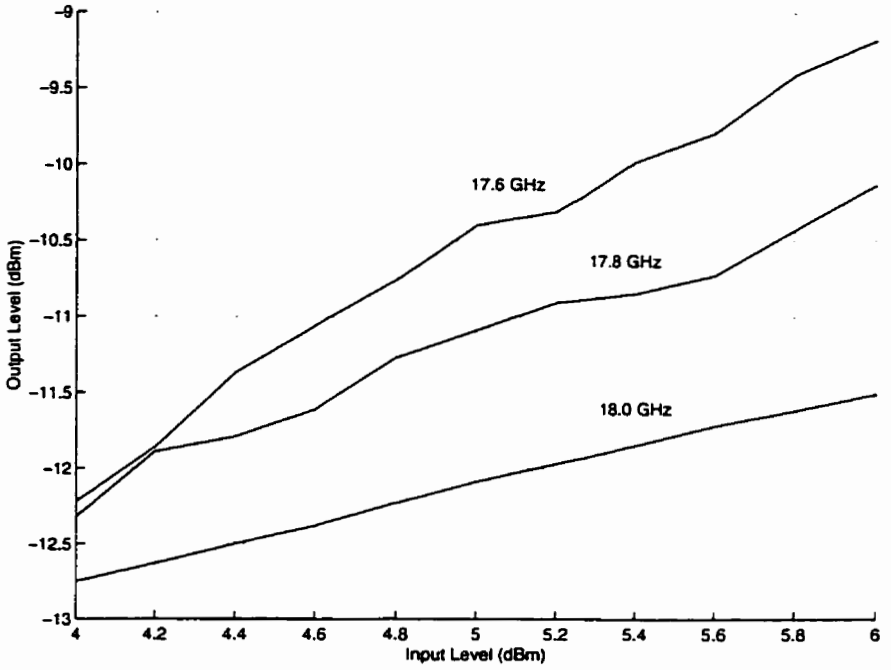


Figure 6.20 Frequency/phase multiplier output level as a function of input level for several different frequencies.

circuit principles to higher frequency implementations. In the next section, the frequency/phase multiplier is combined with the fractional phase shifter to determine the combined performance as a phase shifter/modulator.

6.5 Modulator Performance

The fractional phase shifter and the frequency/phase multiplier were combined and the modulator was tested for a variety of performance parameters. First, the output level as a function of frequency was tested with the combined fractional phase shifter and frequency/phase multiplier to verify the compatibility of the two circuits over the bandwidth of interest. Next, various modulating signals were injected into the fractional phase shifter portion of the modulator, to observe the output passband signal characteristics and the demodulated baseband signal characteristics. Finally, the suitability of the modulator for use with high frequency baseband signals was investigated.

6.5.1 Test Setup

The modulator performance was investigated using the test setup shown in Figure 6.21. The HP8341B synthesized generator was used to provide a stable CW input signal in the range of 3.6 GHz to the fractional phase shifter. The output level of the HP8341B was adjusted until the input level of the frequency/phase multiplier was +5 dBm. The output signal spectrum from the combined fractional phase shifter and frequency/phase multiplier was measured using an HP70000 spectrum analyzer. The multiplier gate and drain bias voltages were set as in the simulations to -3.5 V and +3 V, respectively, for all measurements.

The HP70000 spectrum analyzer was also used as a downconverter to translate the modulated output signal spectrum at 18 GHz to a low frequency IF for demodulation. The frequency span on the HP70000 was set to 0 Hz in this case, to inhibit sweeping and provide a downconverted output signal at a 21.4 MHz auxiliary IF output. This signal was further downconverted to be inside the 10 MHz input bandwidth of the HP89410A vector signal analyzer. The HP89410A was used to provide analog and digital phase coherent demodulation, without requiring a carrier or bit timing reference. This enabled measurements of the modulated signal phase as a function of time and also provided demodulated GMSK signal measurements.

All modulation signals were generated using an HP33120A arbitrary waveform generator. The generator synthesized time waveforms by functioning as a D/A converter, repeatedly cycling through frames of discrete time data points that were loaded into its internal data buffer. The modulation signals were DC biased to the voltage control range of the fractional phase shifter, using the bias circuit shown in Figure 6.22. The 1 kΩ resistor restricts the baseband bandwidth and was included only for current limiting as a precaution during testing, in the event that the varactors were inadvertently forward biased. The resistor was later removed during wideband baseband

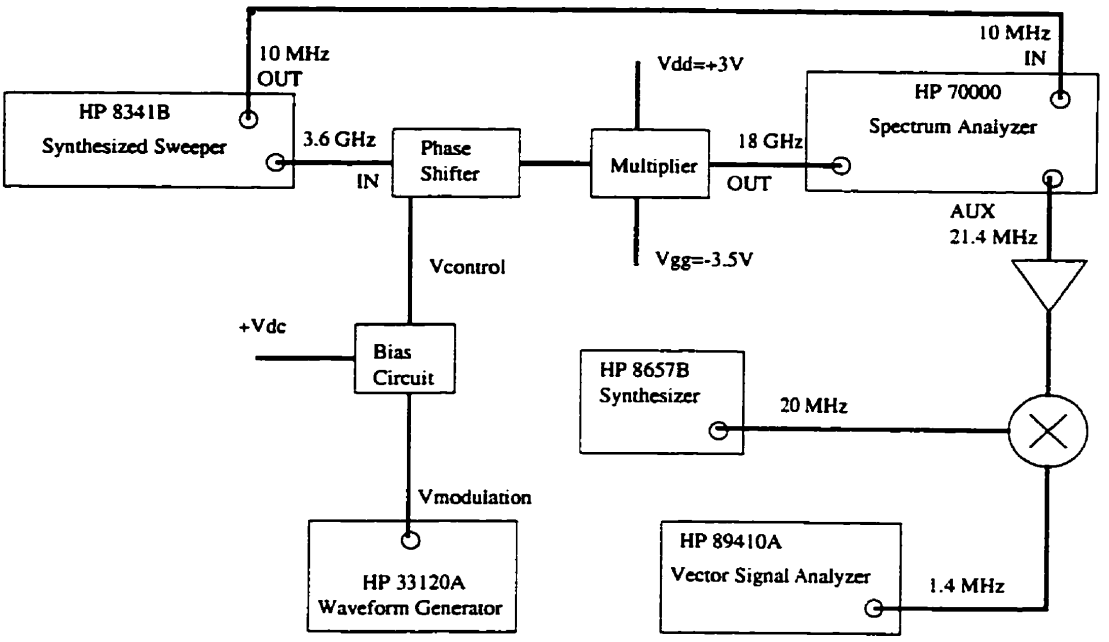


Figure 6.21 Test setup for measuring the 18 GHz modulator performance parameters.

testing.

6.5.2 Measurement Results

Frequency Response

The output level of the modulator as a function of frequency around 18 GHz was measured by slowly sweeping the HP8341B output frequency around 3.6 GHz, with the HP70000 spectrum analyzer trace set in 'hold' mode to store the trace as the HP8341B frequency was swept. The HP8341B output level was increased slightly from the measurements taken with the multiplier alone, to account for the loss through the phase shifter and maintain an input level of +5 dBm to the multiplier. The output level as a function of frequency is shown in Figure 6.23.

Figure 6.23 with the combined phase shifter and multiplier is comparable

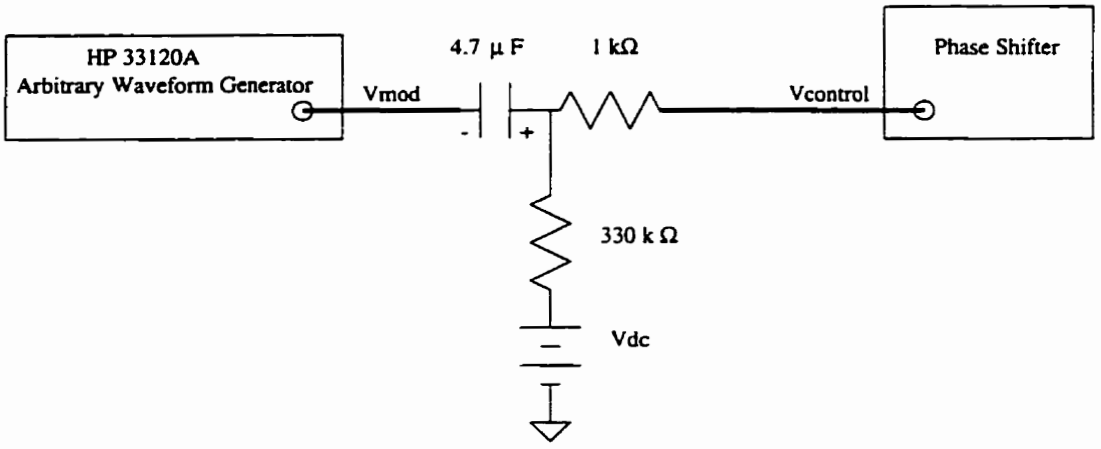


Figure 6.22 Modulation signal DC bias circuit.

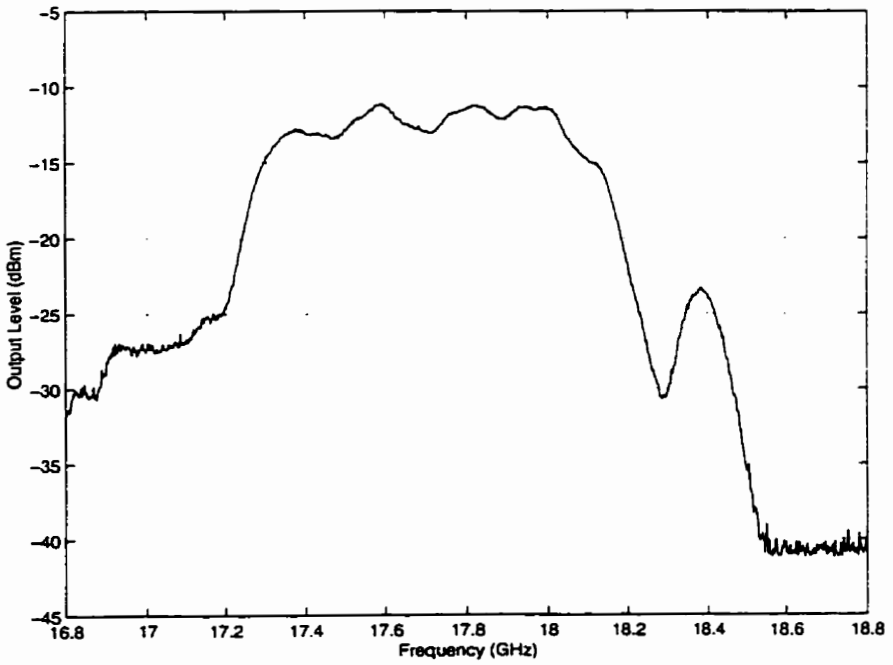


Figure 6.23 Modulator output level as a function of frequency.

to Figure 6.18 with the multiplier alone, suggesting that the two circuits are compatible. The performance is also comparable to that predicted by the simulations of Section 5.4, with the output level approaching -10 dBm in the passband. The passband bandwidth is actually slightly wider than that of the multiplier alone, and is on the order of 700 MHz. This behaviour was also predicted by the simulations of Section 5.4 and suggests that the modulator is appropriate for high rate modulation.

Next, the HP33120A arbitrary waveform generator was used to generate various modulating voltage waveforms, which were injected into the fractional phase shifter portion of the modulator via the bias circuit shown in Figure 6.22.

Serrodyne Modulator

The first modulating signal tested was a 10 kHz sawtooth signal, with voltage waveform shown in Figure 6.24. This modulating signal, when used with a full 360 degree linear phase shifter, results in a serrodyne (or sawtooth) modulator [21][24][32]. The serrodyne modulator operates on the principle of indirect FM, in that a linear increase or decrease in the carrier phase of 360 degrees in a time, T, results in a carrier frequency shift of $\pm 1/T$ Hz from the apparent carrier frequency. This function is extremely useful in providing stable, ultra-small frequency translations in a microwave or millimeter-wave carrier, where the translation frequency is controlled by varying the frequency of the sawtooth modulating signal.

Figure 6.25 shows the output spectrum at an apparent carrier frequency of 17.5 GHz, with the sawtooth modulating signal of Figure 6.24. The peak to peak voltage of the modulating signal is such as to provide full 360 degree phase control. From Figure 6.25, it is apparent that the modulator is performing well in producing the serrodyne modulation function, as the carrier frequency is effectively shifted by 10 kHz with little loss. The levels

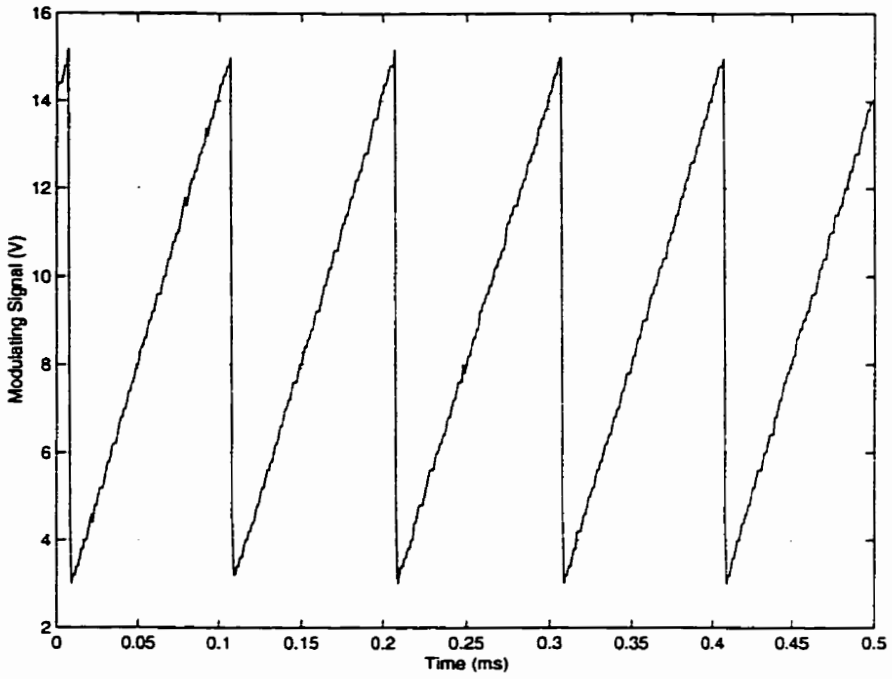


Figure 6.24 Sawtooth modulating signal used to test the serrodyne modulator function.

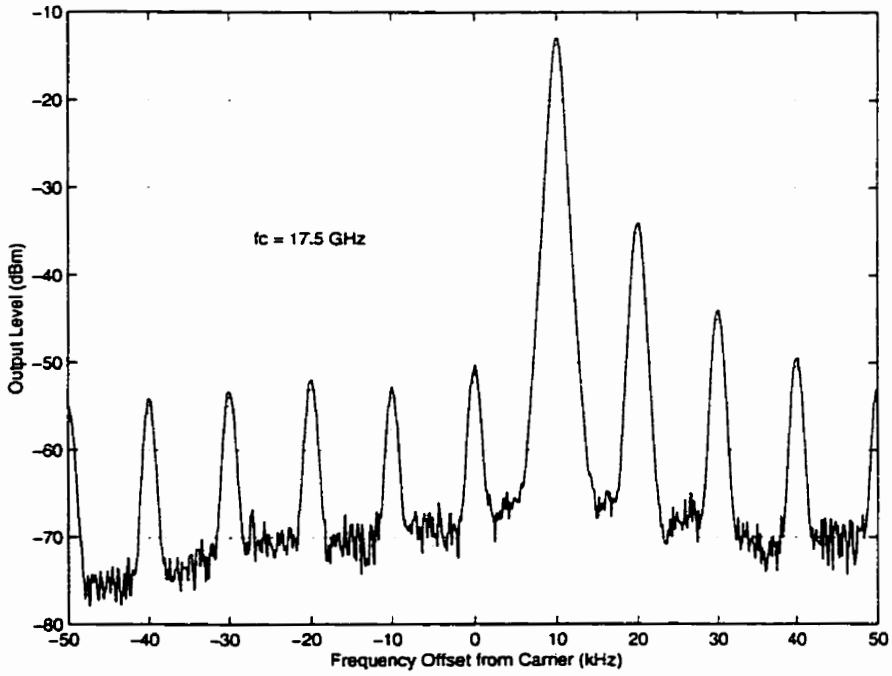


Figure 6.25 Modulator output spectrum with 10 kHz sawtooth modulation.

of the sidebands are also very low. The sidebands are a result of a number of factors, the main contributors being tuning nonlinearity and amplitude modulation [32].

The results of the serrodyne test suggest that the modulator is providing 360 degree linear phase control of the carrier. This test alone, however, is not conclusive in this assumption. Garver [21] reported that the serrodyne function can be realized with acceptable sideband levels using a nonlinear phase modulator with deliberate sawtooth under-modulation. Therefore, an additional test was conducted to verify the phase shift range and linearity of the complete modulator.

Phase Shift Range and Linearity

Measuring the output phase of a 2-port device containing a frequency translation is not a straightforward task using conventional vector network analysis. Most network analyzers, like the HP8510, are tuned for the same input and output frequency, with the output signal providing the phase reference for vector measurements. Therefore, it is difficult to provide a phase coherent reference for the 2-port output signal phase when the input frequency is different then the output frequency. If the output frequency of the 2-port device is a harmonic of the input signal, a coherent phase reference for the output signal can be obtained by using two separate synthesized signal generators, phase locked to a common reference. One generator provides the input signal at a subharmonic of the output frequency and the other generator is set to the output frequency and provides the phase reference.

Another method of obtaining a phase coherent reference signal at the 2-port output frequency is to recover the carrier from the modulated output signal. Carrier recovery is provided by the HP89410A vector signal analyzer, operating in analog phase demodulation mode. Provided that the modulating signal is balanced to provide both positive and negative phase shift from

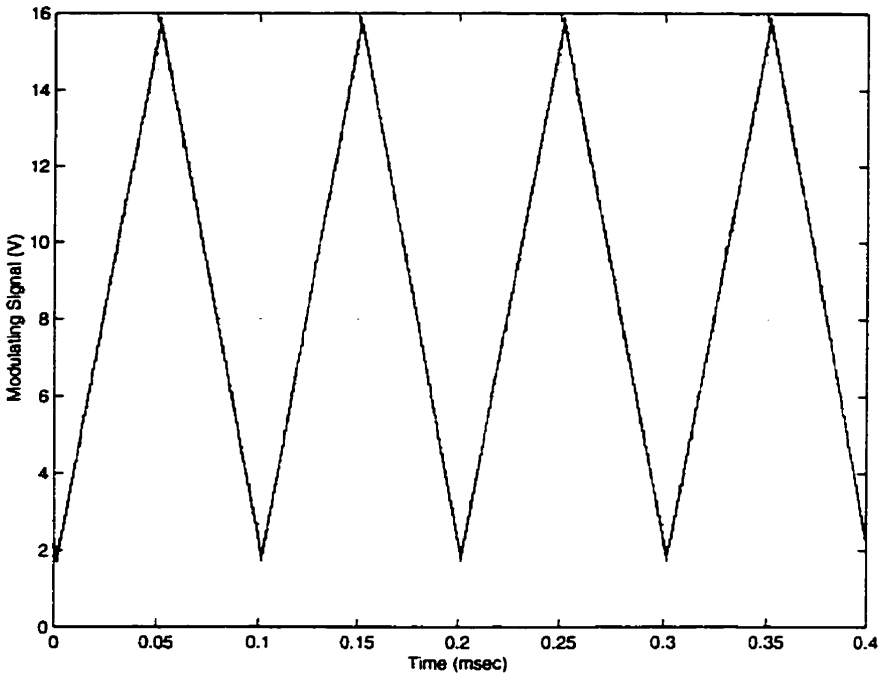


Figure 6.26 Triangle wave modulating signal used to verify the modulator phase shift range and linearity.

the nominal carrier signal phase, the demodulated signal phase shift as a function of time can be displayed on the HP89410A. This is the measurement technique that was used to verify the modulator phase shift range and linearity.

A CW carrier signal was input to the modulator at 3.53 GHz, producing an output signal at 17.65 GHz. The 17.65 GHz output signal was downconverted as described above and input to the HP89410A. A 10 kHz triangle wave modulating signal, shown in Figure 6.26, was injected into the modulator to verify the phase shift range and linearity. The peak to peak voltage of the triangle wave modulating signal is large enough to cover the full phase control range of the modulator. The triangle wave is an appropriate test signal for this measurement, as it produces both positive and negative carrier phase shift and a balanced modulated output signal spectrum about the carrier, as shown in Figure 6.27 for the downconverted output spectrum.

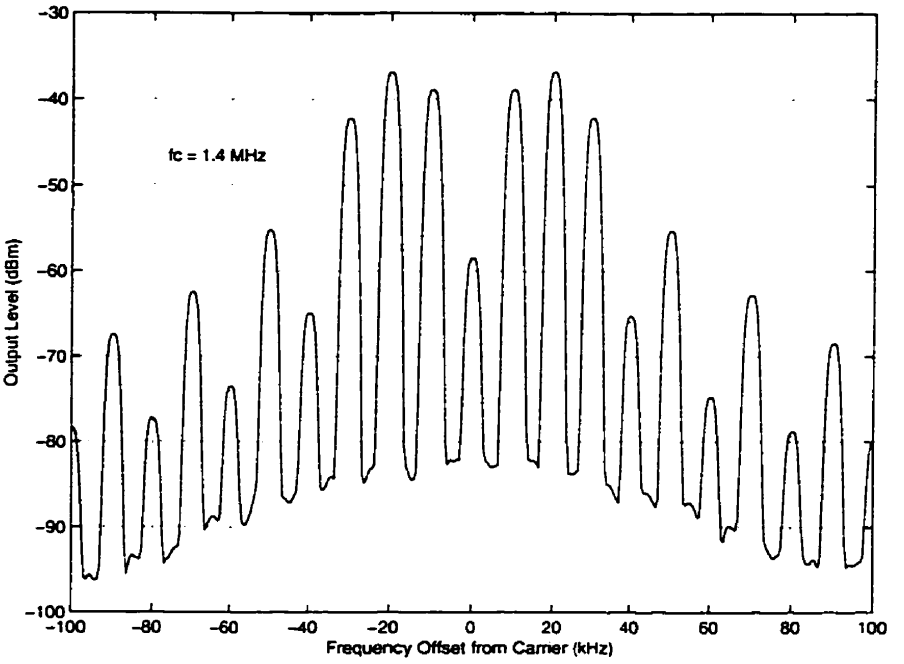


Figure 6.27 Modulator output spectrum with 10 kHz triangle wave modulating signal.

The demodulated carrier excess phase as a function of time is shown in Figure 6.28, for the 10 kHz triangle wave modulating signal. From Figure 6.28, the phase shift range is observed to be $\pm$ 180 degrees, and the waveform is very similar to the triangle wave modulating signal shown in Figure 6.26. The apparent flattening of the peaks of the demodulated triangle wave phase in Figure 6.28 is a result of insufficient sampling points per cycle to resolve the true peaks of the triangle wave. One half cycle of the demodulated triangle wave excess phase was "flattened" mathematically to remove the linear component as a function of time and assess the modulator phase shift linearity. The phase shift linearity for a flattened portion of the excess phase waveform of Figure 6.28 is shown in Figure 6.29, with straight line interpolation between the measured points. The phase error of 5 degrees shown in Figure 6.29 is on the order expected from the results of the fractional range shifter and verifies that the complete modulator is providing full 360 degree linear phase control of the carrier.

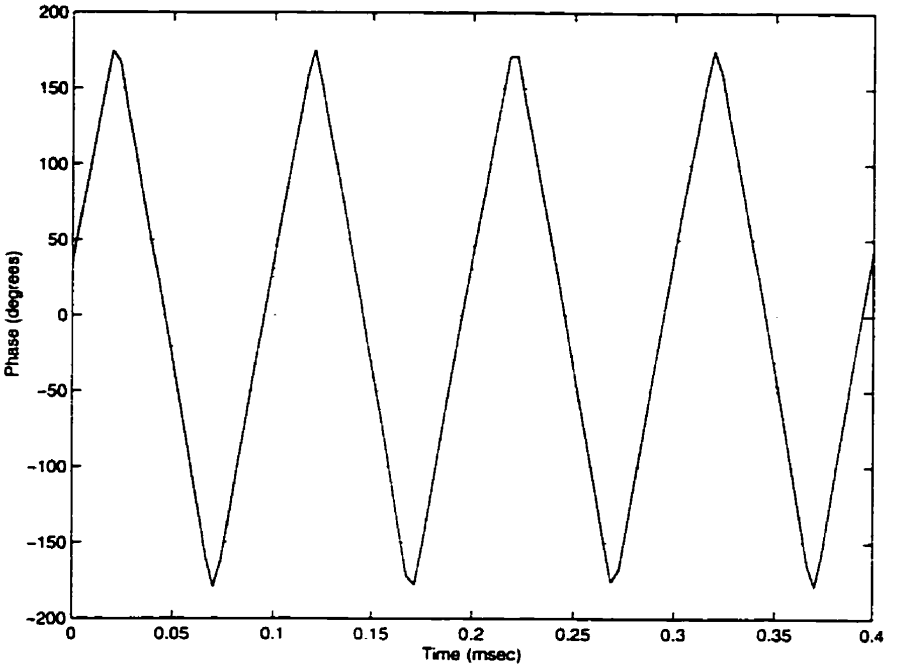


Figure 6.28 Demodulated carrier excess phase as a function of time for a 10 kHz triangle wave modulating signal.

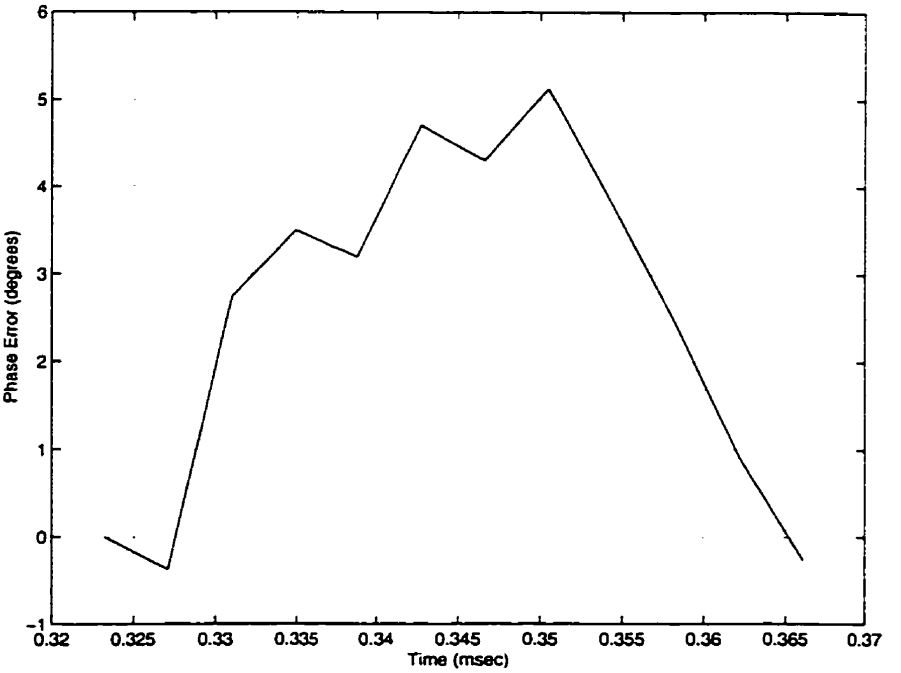


Figure 6.29 Demodulated carrier excess phase error over the modulator phase control range.

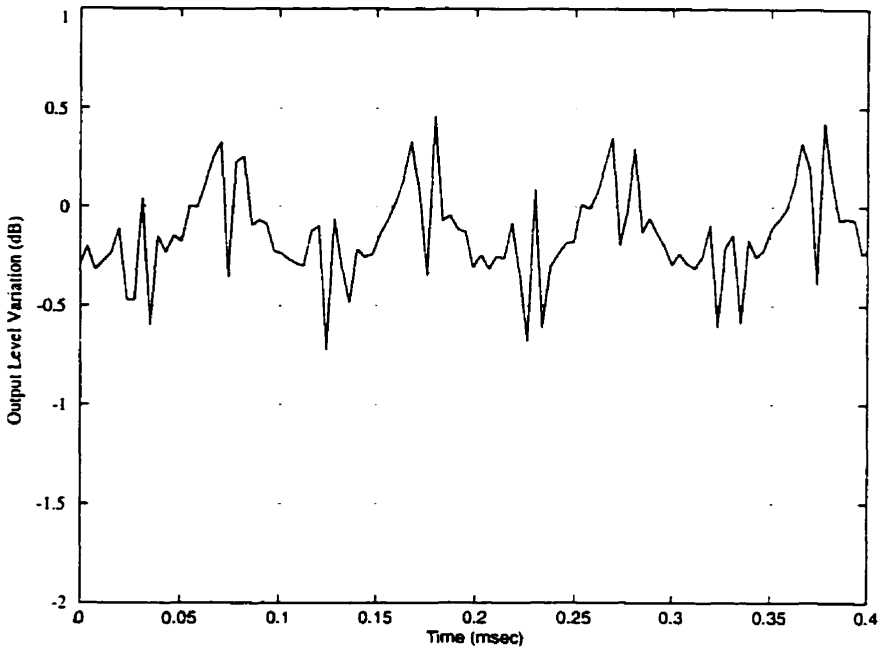


Figure 6.30 Carrier amplitude variation over the modulator phase control range.

The modulated output signal amplitude variation as a function of time over the full phase control range was also measured with the HP89410A, using the triangle wave modulating signal shown in Figure 6.26. The modulated output signal amplitude variation as a function of time, shown in Figure 6.30, is within 1 dB, proving the modulator is providing good constant envelope modulation.

MSK Demodulation

The HP89410A was set in coherent MSK digital demodulation mode, to demodulate the downconverted 17.65 GHz triangle wave phase modulated signal. As the triangle wave modulates the carrier over the full 360 degree phase range, and in both directions for one cycle of the triangle waveform, all phase states in the MSK constellation diagram are visited twice in each modulation cycle. Therefore, the demodulation symbol rate was set to 80 kbps, or 8× the triangle wave modulation frequency, for the 8 symbols encountered

during the triangle wave modulation cycle. Figure 6.31 shows the demodulated inphase (I) and quadrature (Q) "eye" diagrams over a two symbol interval for 200 demodulated symbols, as well as the modulation vector and symbol constellation diagrams in vector signal space for 200 demodulated symbols. All diagrams are normalized to a unit magnitude.

The eye diagrams in Figure 6.31 show very little intersymbol interference (ISI) and are very close to the ideal sinusoidal waveforms expected for MSK, as described in Section 2.1. The modulation vector diagram of Figure 6.31c represents the carrier amplitude and phase modulation trajectory as a function of time. The ideal vector diagram for MSK, which is a constant envelope continuous phase modulation, is a circle in vector signal space with unit magnitude. The vector diagram of Figure 6.31 confirms that there is very little carrier amplitude variation and 360 degree continuous phase modulation, as the vector diagram is very close to the ideal unit circle. The constellation diagram of Figure 6.31d demonstrates that the demodulated symbols line up very well with the ideal symbol points, which are represented by crosses.

The performance of the modulator is very encouraging, and proves that the modulator is effectively providing 360 linear phase modulation of a carrier at 18 GHz. The next step was to subject the modulator to random baseband Gaussian prefiltered modulation signals.

GMSK Modulation

The effectiveness of the modulator in providing GMSK modulation at 17.65 GHz was verified. The HP33120A arbitrary waveform generator was used to generate phase control signals representative of random, Gaussian prefiltered baseband input data. The HP33120A data buffer was loaded with 8192 points of computer generated, Gaussian prefiltered, discrete time data, representing 128 random data symbols with 64 data points per symbol. The HP33120A was set to continuously cycle through this frame of data and

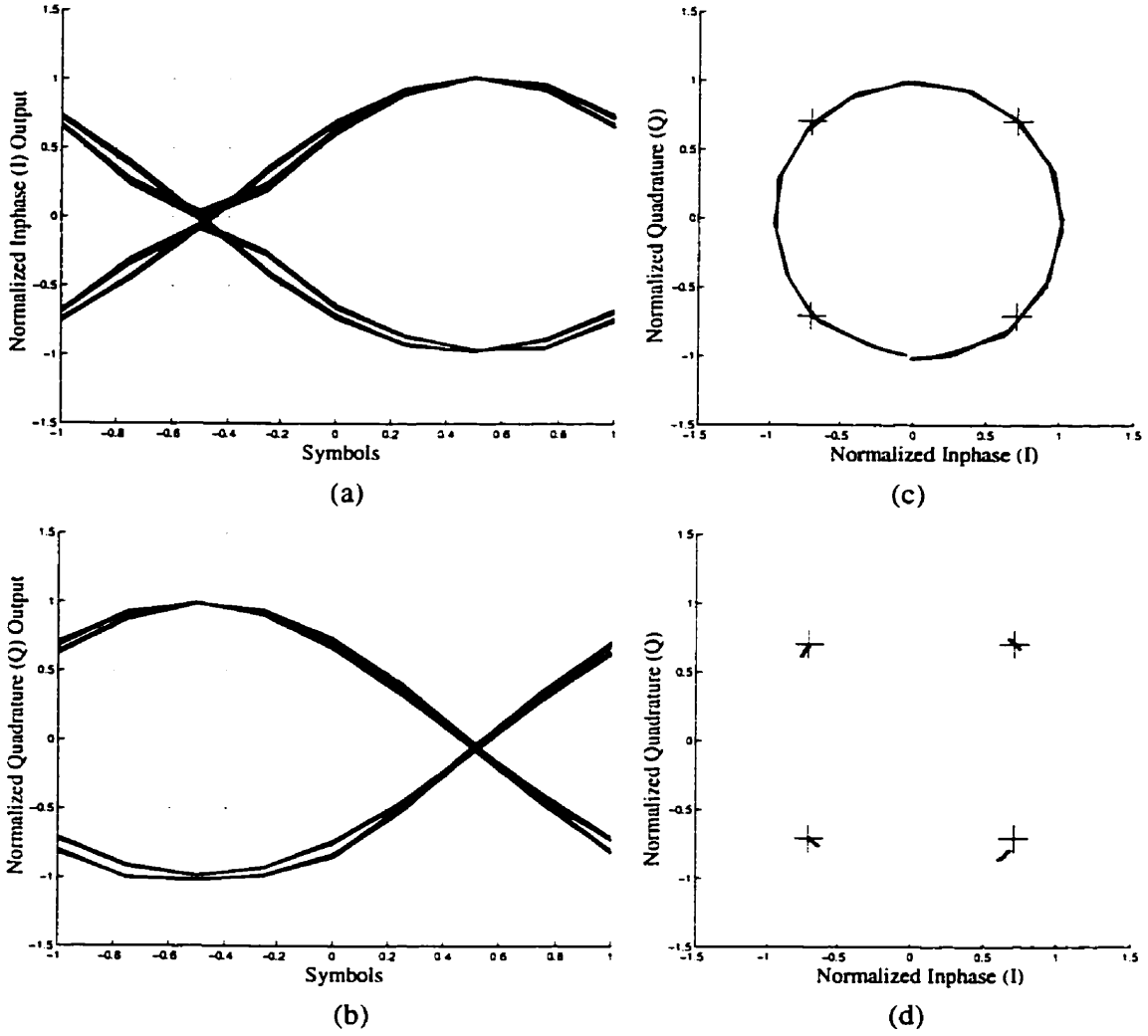


Figure 6.31 MSK demodulated signal characteristics of triangle wave modulated carrier signal at 17.65 GHz: (a) Inphase Eye; (b) Quadrature Eye; (c) Vector; (d) Constellation.

provide a continuous analog output modulation signal. With this method of generation, the data is cyclic and not truly random. It is random enough, however, to provide an accurate representation of random signal modulation characteristics for measurement purposes. The modulation signals were DC biased to the voltage control range of the fractional phase shifter, using the bias circuit shown in Figure 6.22.

The input modulation signals used for testing are shown in Figure 6.32, for normalized Gaussian premodulation filter bandwidths, BT_b, of ∞ (MSK), 0.5, 0.3, and 0.2. As shown in Figure 6.32, the Gaussian filtering must be applied to the modulating signal before the the signal is wrapped to account for the $\pm\pi$ voltage discontinuity, to avoid the incorrect application of Gaussian filtering to the wrapping discontinuity. The input symbol rate was set to 80 kHz, as was used for the triangle wave modulation measurements, and the peak to peak voltage of the modulating signal was adjusted to encompass the full phase shift range of the modulator.

The GMSK modulated output spectra at 17.65 GHz are shown in Figure 6.33 for the various modulating signals of Figure 6.32. The modulated signal spectra are well balanced about the carrier frequency of 17.65 GHz, which indicates good phase control linearity for both increasing and decreasing phase control signals. The effect of the Gaussian premodulation filter in limiting the spectral sidelobe levels is clearly evident from Figure 6.33.

The HP89410A was set in coherent MSK digital demodulation mode, to demodulate the downconverted 17.65 GHz GMSK modulated signals shown in Figure 6.33. Figures 6.34 to 6.37 show the demodulated I and Q eye diagrams over a two symbol interval for 200 demodulated symbols, as well as the modulation vector and symbol constellation diagrams in vector signal space for 200 demodulated symbols. All diagrams are normalized to a unit magnitude.

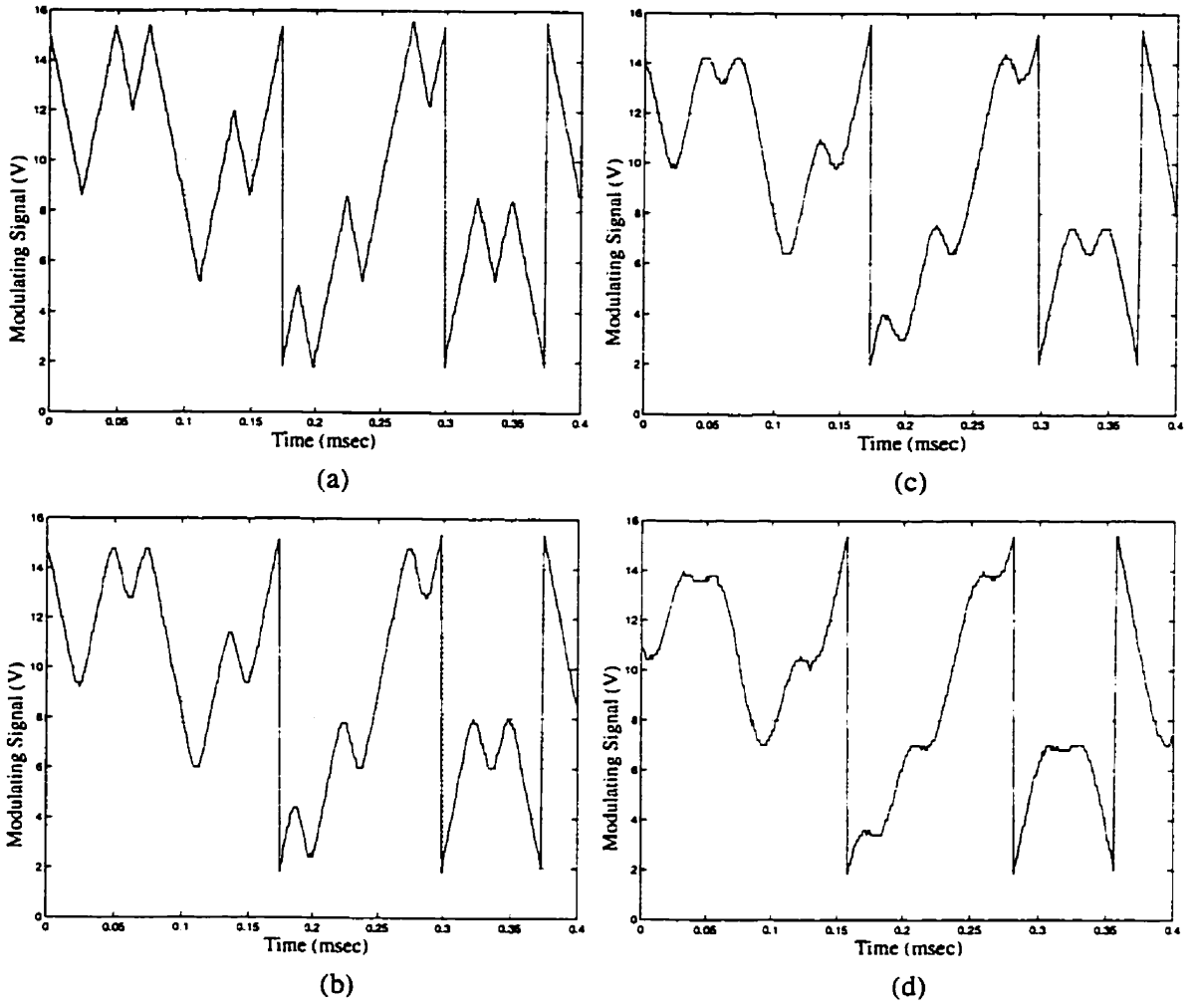


Figure 6.32 Modulation signals representing random base-band data: (a) Unfiltered (MSK); (b) 0.5 GMSK; (c) 0.3 GMSK; (d) 0.2 GMSK.

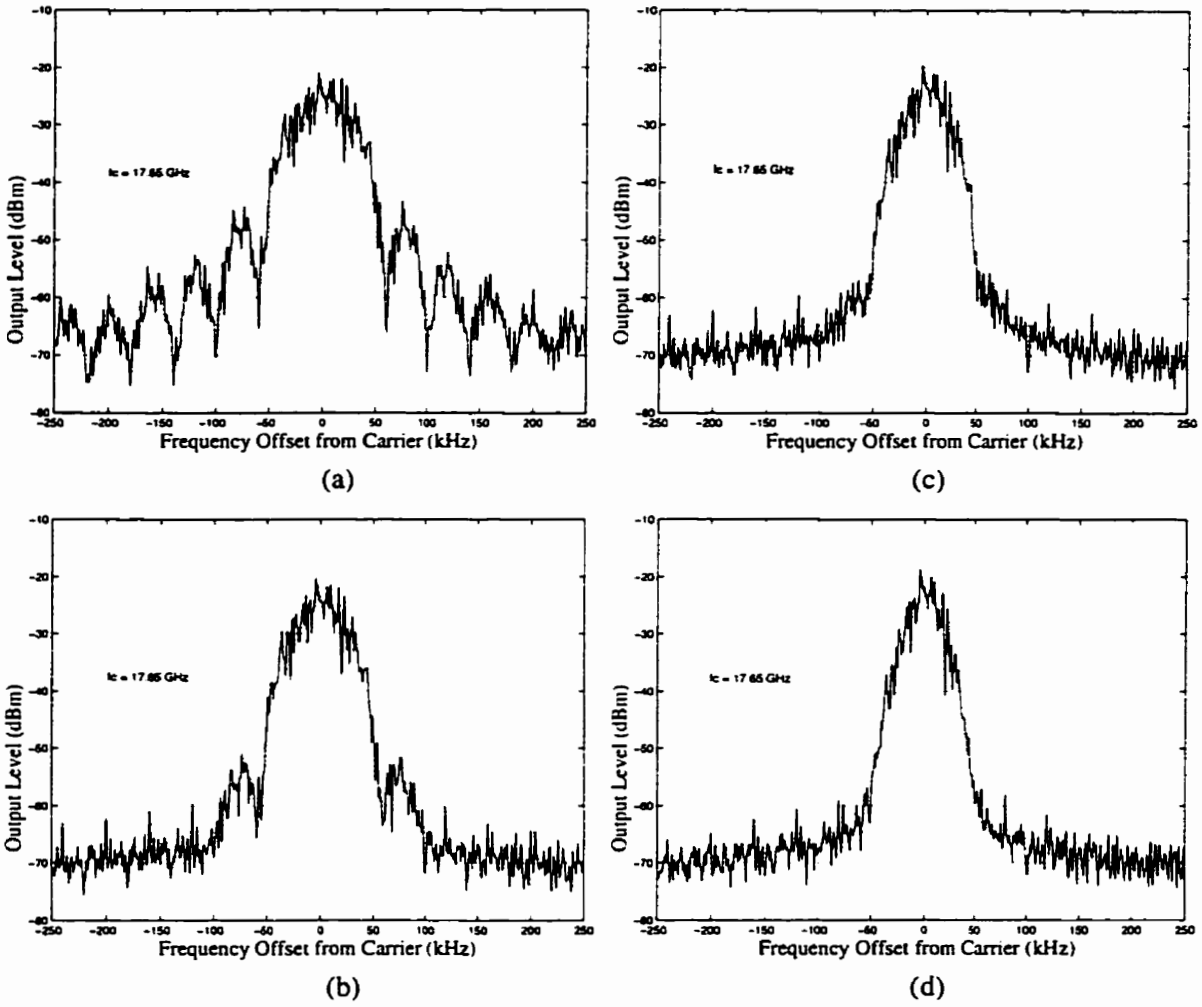


Figure 6.33 Modulated output signal spectrum at 17.65 GHz: (a) Unfiltered (MSK); (b) 0.5 GMSK; (c) 0.3 GMSK; (d) 0.2 GMSK.

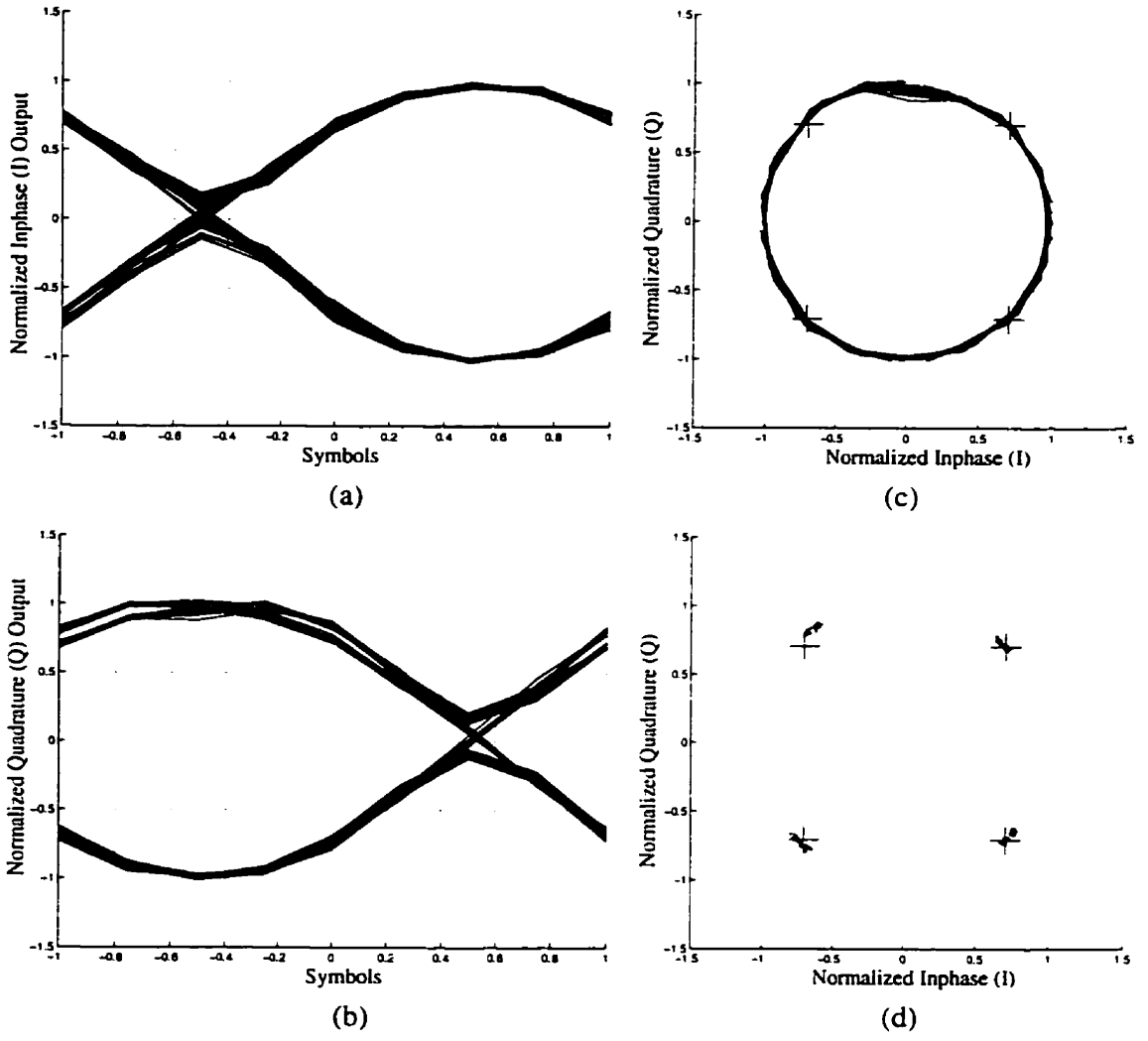


Figure 6.34 Coherent demodulation of MSK modulated carrier signal at 17.65 GHz: (a) Inphase Eye; (b) Quadrature Eye; (c) Vector; (d) Constellation.

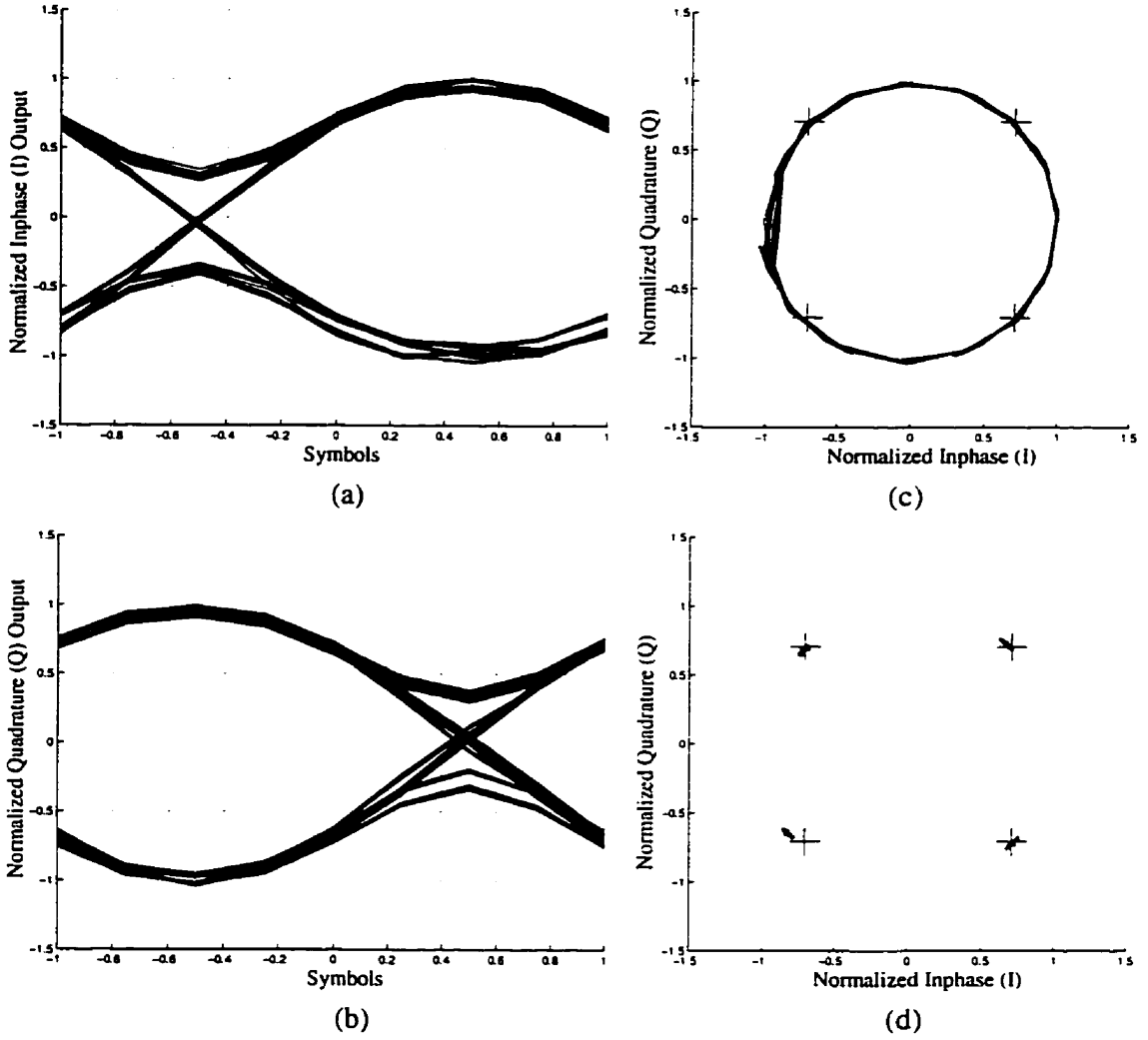


Figure 6.35 Coherent demodulation of 0.5 GMSK modulated carrier signal at 17.65 GHz: (a) Inphase Eye; (b) Quadrature Eye; (c) Vector; (d) Constellation.

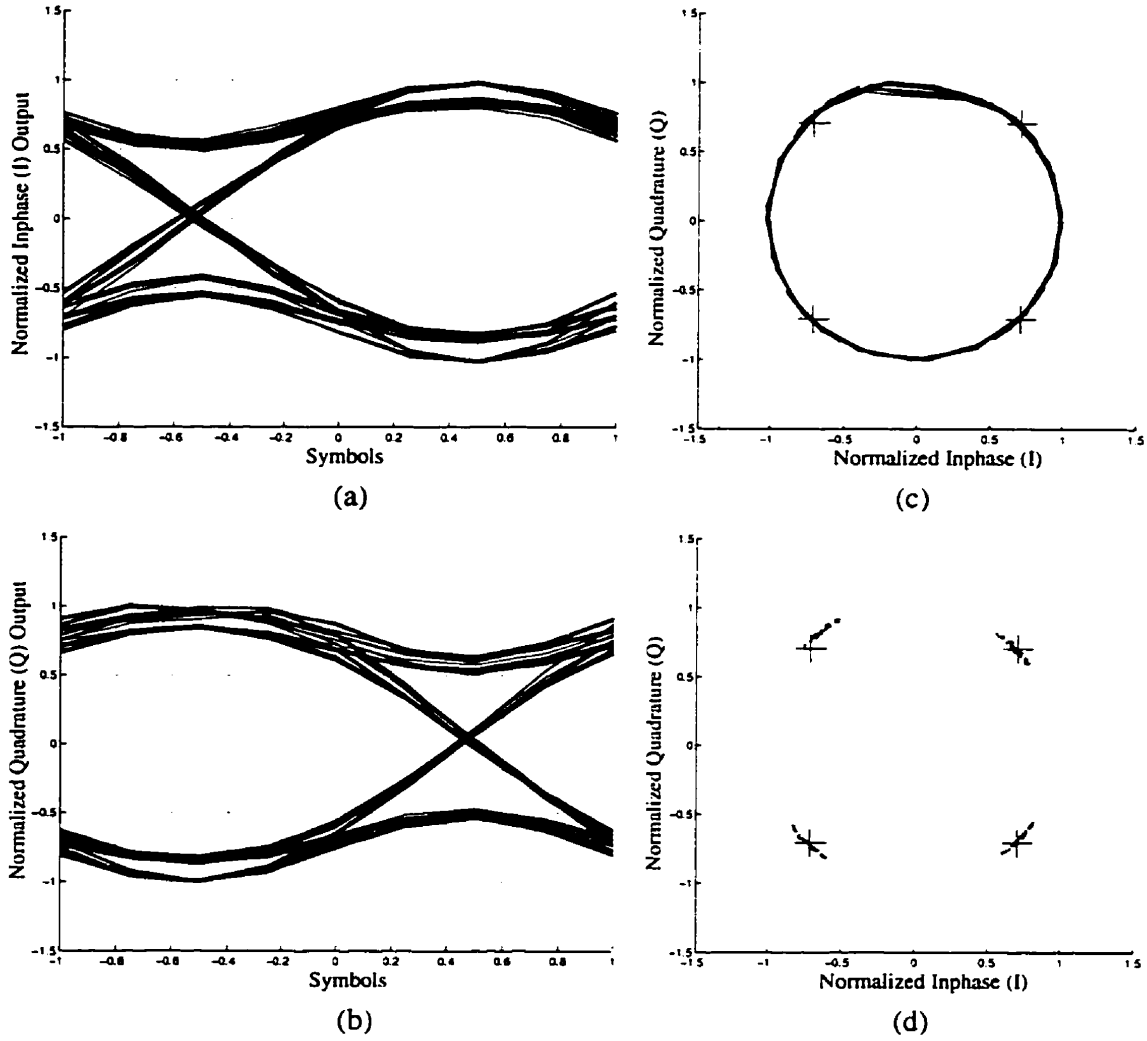


Figure 6.36 Coherent demodulation of 0.3 GMSK modulated carrier signal at 17.65 GHz: (a) Inphase Eye; (b) Quadrature Eye; (c) Vector; (d) Constellation.

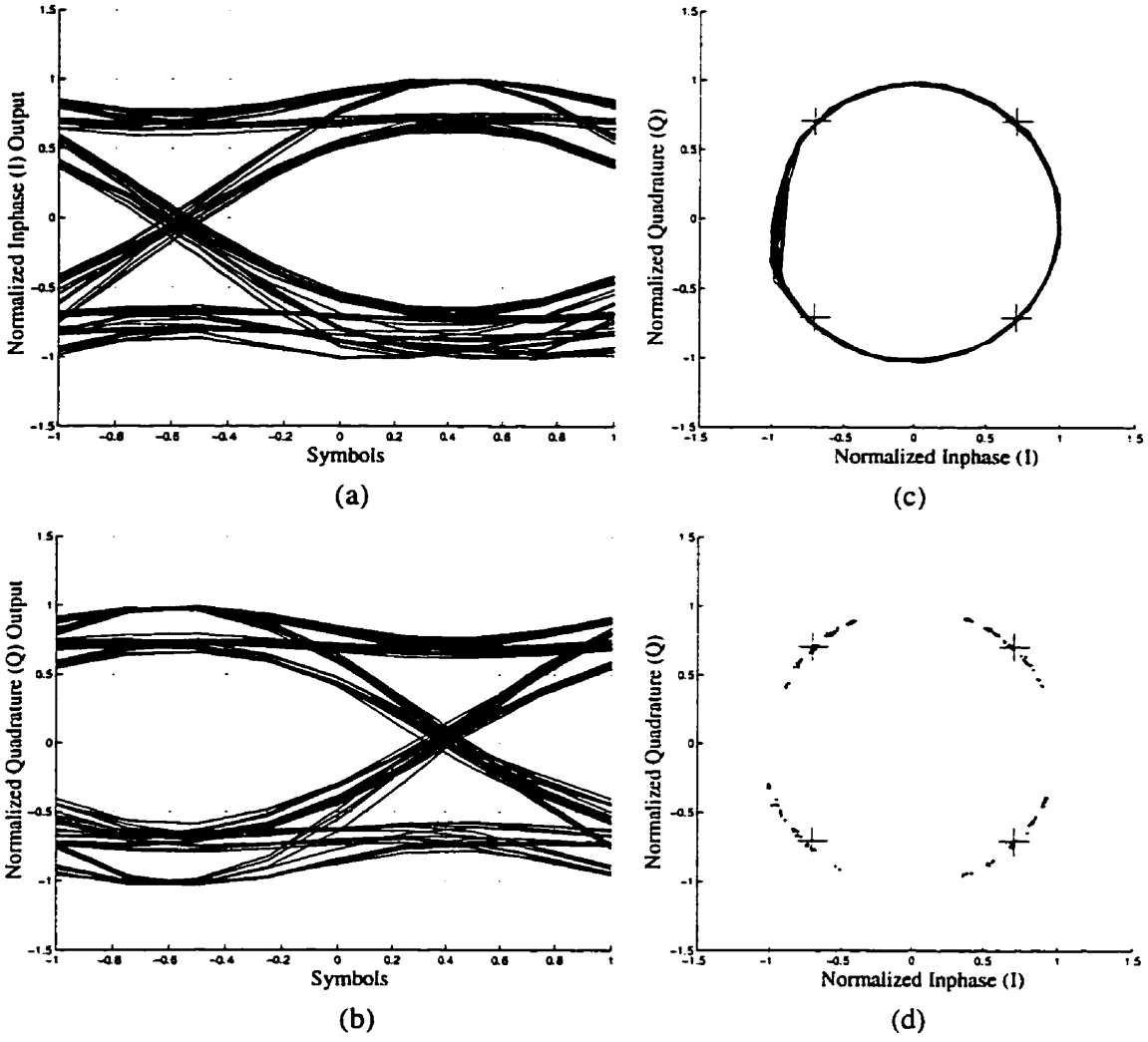


Figure 6.37 Coherent demodulation of 0.2 GMSK modulated carrier signal at 17.65 GHz: (a) Inphase Eye; (b) Quadrature Eye; (c) Vector; (d) Constellation.

The demodulated MSK signal characteristics shown in Figure 6.34 are comparable to the demodulated triangle wave signal characteristics of Figure 6.31, verifying that the modulator is accurately responding to random phase state transitions through the excess phase trellis. Figures 6.35 to 6.37 are comparable to the ideal results of Section 2.1, and demonstrate the effect of the Gaussian premodulation filter in the demodulated output signal characteristics. As the filter baseband bandwidth, BT_b, is reduced, the modulated output signal spectrum becomes more compact, at the expense of increased ISI in the demodulated time signal. This is clearly seen from the I and Q diagrams of Figures 6.35 to 6.37, where the peak to peak amplitude of the eyes at the zero crossing points (-0.5 symbols for I, +0.5 symbols for Q) increases and the peak to peak amplitude of the eyes at the maximum points (0.5 symbols for I, -0.5 symbols for Q) decreases, as BT_b is reduced. Coherent demodulation with this increased ISI is still possible, provided that the I and Q waveforms are sampled at $T_b/2$, or at a symbol position of 0 as shown in the figures, corresponding to phase states of ± 45 and ± 135 degrees in vector signal space.

These measurements prove that the proposed modulator can effectively and simply realize GMSK modulation at 18 GHz, using prefiltered baseband modulation signals to continuously control the phase of the carrier over the full 360 degree range. In the next section, the modulator bandwidth is investigated, and some factors which limit the high speed operation of the modulator are discussed.

High Speed Modulation

The generation of pure MSK, as described and measured above, is not practical for high speed modulation with this method, due to the high baseband bandwidth required to synthesize the sharp phase transitions in the MSK modulated carrier. Fortunately, most practical radio applications do

not use pure MSK anyway, and employ some degree of Gaussian prefiltering to improve the bandwidth efficiency with the intent of removing the sharp phase transitions in the MSK modulating signal. Providing that the inherent baseband circuit bandwidth is greater than the desired Gaussian filter bandwidth, the Gaussian prefiltering reduces the baseband bandwidth requirement to the order of BT_b, suggesting that the modulator should support very high rate operation.

Unfortunately, the situation is complicated by the phase wrapping problem at the $\pm\pi$ phase point in the carrier excess phase, which is accounted for in the modulating signal by a voltage discontinuity from V_{max} to V_{min} at the voltage control port. This phase transition point is an undesired transition in the GMSK excess phase, and is purely a necessity of implementation since the control voltage cannot go unbounded. Ideally, the voltage transition should occur instantaneously to have no effect on the carrier excess phase.

Practically, the voltage transition cannot happen instantaneously, and is filtered by the inherent lowpass characteristic of the baseband modulation circuit. The lowpass characteristic can be considered as an RC lowpass filter, consisting mainly of the baseband modulation circuit driving impedance and the fractional phase shifter reverse biased varactor capacitance. To further complicate matters, the varactor capacitance is a function of bias. Therefore, the lowpass characteristic is a function of bias and results in different filtering characteristics at the top and bottom of the voltage control range. The effect of the inherent circuit lowpass characteristic on the $\pm\pi$ voltage discontinuity is demonstrated in Figure 6.38.

The solid trace in Figure 6.38 expands the $\pm\pi$ voltage discontinuity for the 80 kbps 0.5 GMSK modulating signal of Figure 6.32b. The dashed line demonstrates the effect on the modulating signal at the voltage discontinuity when the bit rate is increased to 800 kbps. The normalized time scale in Figure 6.38 represents 1 μsec for the 800 kbps modulating signal and 10 μsec

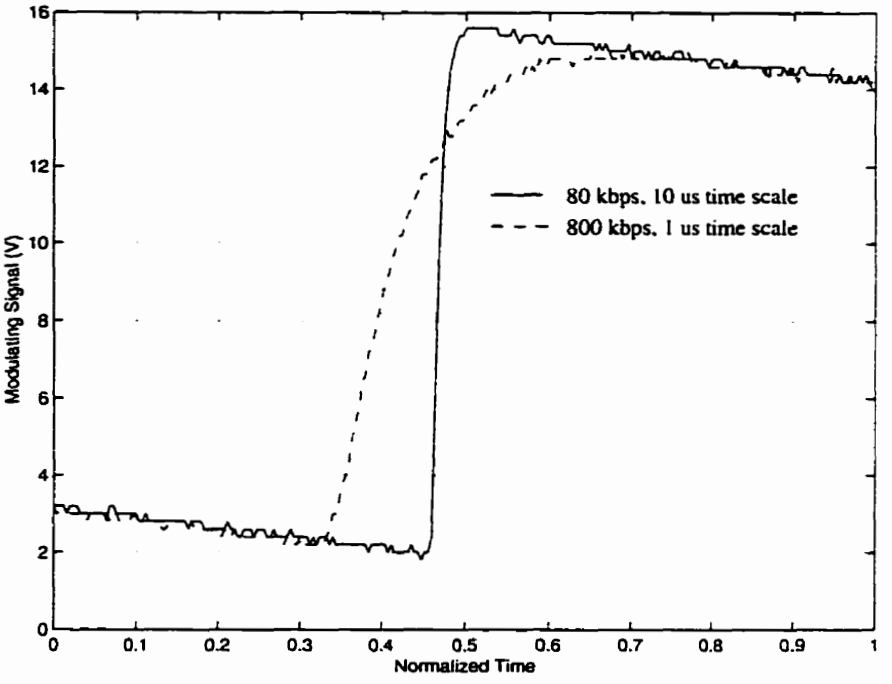


Figure 6.38 Effect of the circuit lowpass characteristic on the $\pm\pi$ voltage discontinuity.

for the 80 kbps modulating signal. For both measurements in Figure 6.38, the 1 kΩ series current limiting resistor was retained in the bias circuit of Figure 6.22, to reduce the circuit lowpass cutoff frequency and enhance the circuit filtering effect for illustrative purposes.

Ideally, the carrier phase at the $\pm\pi$ voltage discontinuity is continuous. The circuit filtering on the voltage control signal, demonstrated in Figure 6.38, imposes an undesired carrier excess phase transition at the $\pm\pi$ signal point in vector signal space. This transition has a smooth trajectory with a fractional bit period duration, and endpoints at less than $\pm\pi$ in vector signal space. Figure 6.39 shows the circuit filtering effect on the demodulated signal characteristics. The undesired phase trajectory is reflected in Figure 6.39c as a collapse in the modulation vector diagram around the $\pm\pi$ excess phase point and distortion in the eye diagrams at the 0.5 symbol point.

The increased distortion in the demodulated signals does not necessarily

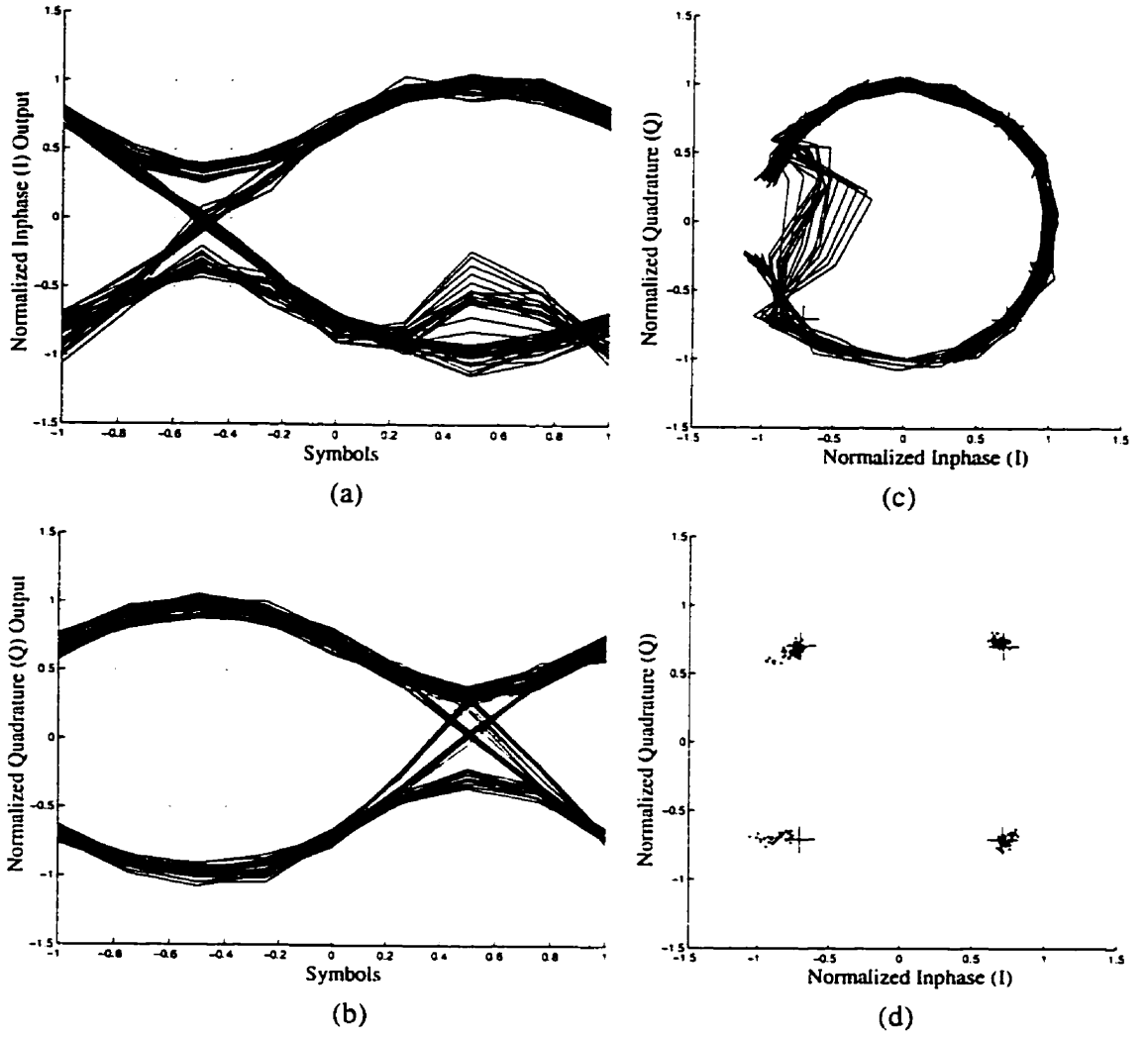


Figure 6.39 Coherent demodulation of 0.5 GMSK modulated carrier signal with $\pm\pi$ voltage discontinuity filtering effect: (a) Inphase Eye; (b) Quadrature Eye; (c) Vector; (d) Constellation.

inhibit coherent demodulation, since the symbol points are sampled midway through the bit interval. Therefore, even with the large distortion at the $\pm\pi$ excess phase point caused by the circuit filtering, the signal constellation diagram shown in Figure 6.39d is still quite good, as the pattern averaged excess phase trajectory does not deviate significantly from that of GMSK. In other words, as long as the filtering effect is small enough to maintain the endpoints of the unwanted phase trajectory between $\pm\pi$ and the symbol sampling point of $\pm$ 135 degrees, coherent demodulation is possible. This excess phase trajectory behaviour is not unlike the reduction in phase trajectory over the bit interval caused by Gaussian lowpass filtering. The fact that the phase trajectory over the bit interval is not excessively reduced is the reason that the Gaussian prefiltered phase can be coherently demodulated.

Gaussian lowpass filtering results in a modulated signal which preserves a nearly constant amplitude envelope. The inherent baseband filtering effect at the $\pm\pi$ voltage discontinuity does not support this property, and the result is variation in the modulated signal amplitude envelope around the $\pm\pi$ phase point, which is apparent from the modulation vector diagram in Figure 6.39c.

The envelope variation in CPM modulated signals such as GMSK is not as problematic as with linear modulation methods carrying information in the amplitude of the carrier. These methods rely on linear amplification to maintain low distortion and low spectral spreading in the modulated signal. Nonlinear amplification of the modulated signal of Figure 6.39 will likely tend to restore the sharp phase transition at the $\pm\pi$ voltage discontinuity, reduce the envelope variation, and may even improve the performance. Better amplitude hard-limiting, which is an extreme example of amplifier nonlinearity, from the frequency/phase multiplier would likely reduce the envelope variation associated with the unwanted phase trajectory. The effect of hard-limiting is demonstrated in Figure 6.40 which shows the demodulated signal characteristics with hard-limiting applied numerically to the demodulated I

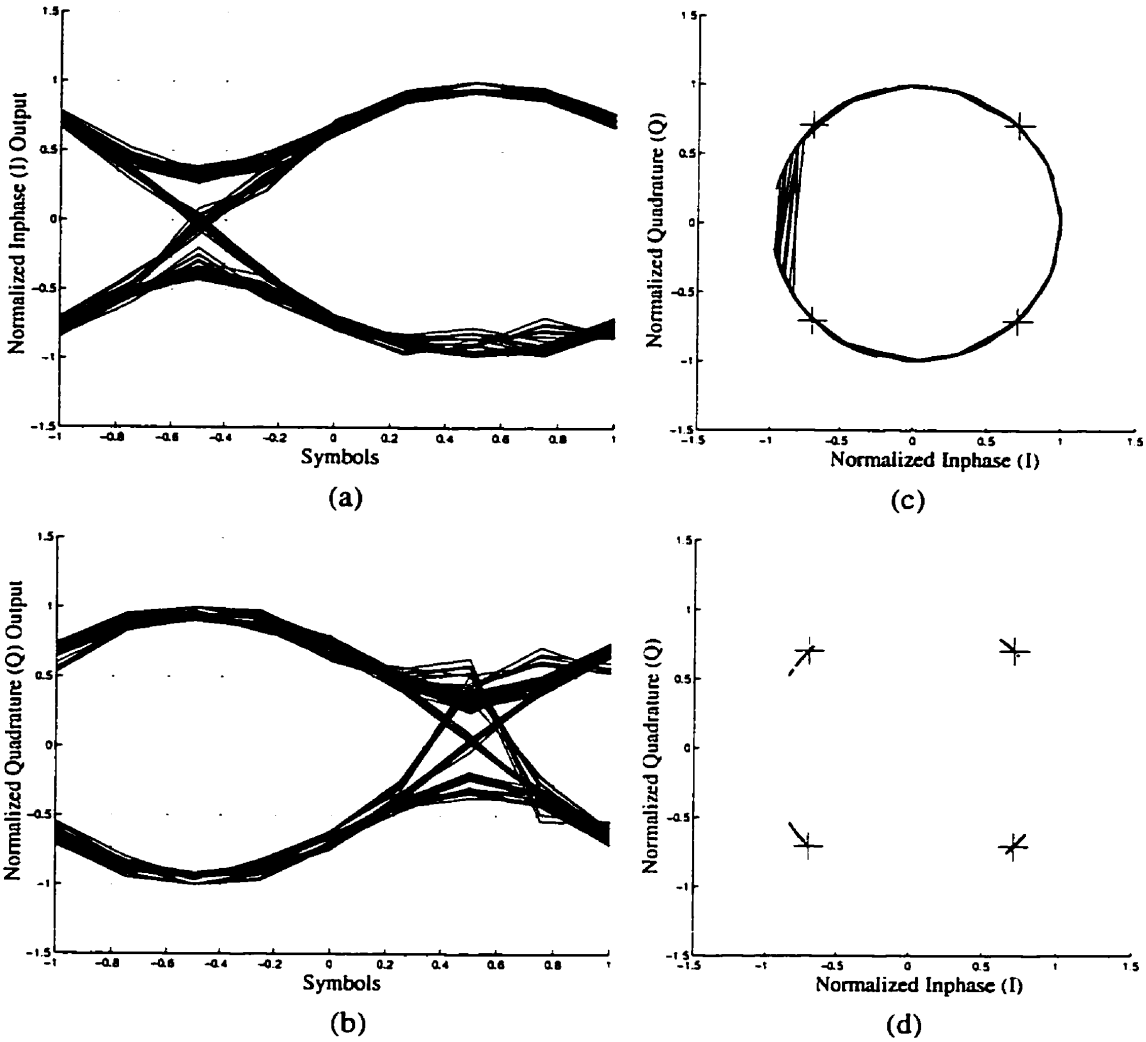


Figure 6.40 Coherent demodulation with numerical hard-limiting to improve the $\pm\pi$ voltage discontinuity filtering effect: (a) Inphase Eye; (b) Quadrature Eye; (c) Vector; (d) Constellation.

and Q data measured in Figure 6.39. This situation is somewhat artificial, as the measured data was adjusted numerically to have constant amplitude envelope, rather than hard-limiting the modulated signal prior to demodulation. Figure 6.40 does demonstrate, however, that improvement in the demodulated signal characteristics can be expected with hard-limiting, and the results more closely resemble the demodulated signal characteristics of Figure 6.35 with little circuit filtering effect.

To summarize, the inherent circuit filtering characteristic effects the control signal response time at the $\pm\pi$ voltage discontinuity and is a limiting factor in the modulator operating rate. Under the frequency limitations of the baseband test setup and modulation signal generation used for this performance verification, acceptable performance was observed at data rates as high as 4 Mbps with the 1 kΩ current limiting resistor removed. This lends much confidence in the feasibility of the proposed modulation method for high data rate operation. Figure 6.41 shows the 0.5 GMSK modulated output spectrum at 17.65 GHz for a 4 Mbps modulating signal and Figure 6.42 shows the demodulated signal characteristics for a 4 Mbps modulating signal.

The artifacts of the circuit filtering limitations discussed above are apparent from Figure 6.42, but the performance is still reasonably good. More amplitude variation in the modulation vector diagram is observed, which is likely a combination of circuit filtering effects at the Gaussian filtered phase transitions, and vector modulation analyzer input bandwidth limitations. With a properly designed, high speed modulation generator having low output driving impedance, fast response time, and a short transmission line connection to the modulator phase control port, it is expected that modulation rates in excess of 20 Mbps are feasible. This assumption is supported by measurements of the baseband bandwidth discussed in the next section.

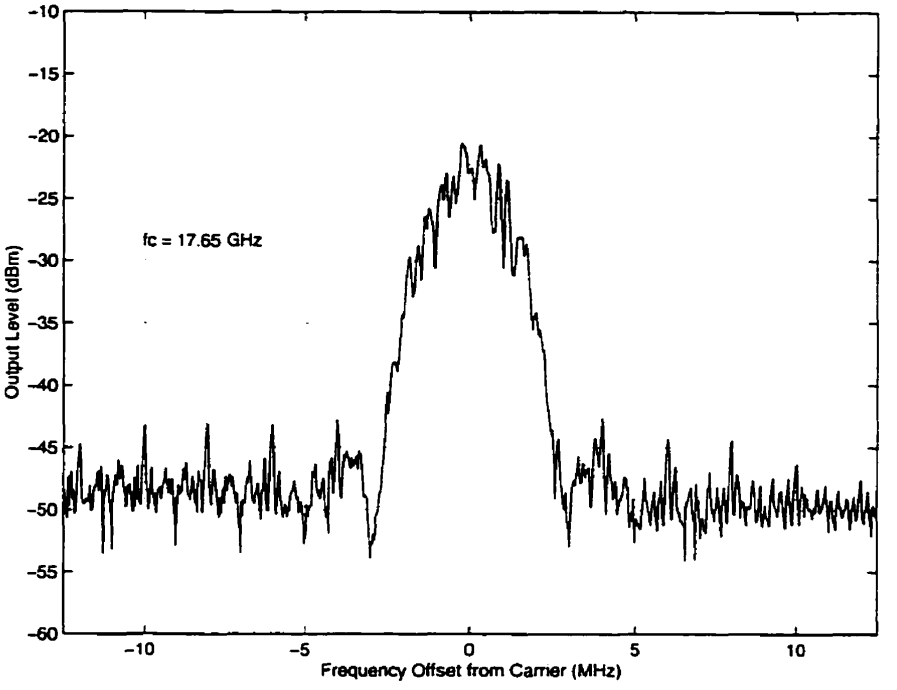


Figure 6.41 Output signal spectrum at 17.65 GHz for a 4 Mbps, 0.5 GMSK modulated carrier.

Modulator Bandwidth

The bandwidth of the modulator was determined using sinusoidal modulating signals, due to difficulties in synthesizing high data rate control signals with available test equipment. Since the modulator provides 360 degree linear phase control of the carrier, analog modulation signals are appropriate for gauging the modulator bandwidth. This is not entirely straightforward, however, as phase modulation is a nonlinear modulation technique. Thus, the baseband modulation signal is not linearly transfered to the carrier in the passband and the baseband and passband bandwidths are not generally comparable. Therefore, in order for the sinusoidal modulating signals to be representative of the useful modulation bandwidth for GMSK modulating signals, the baseband modulation and passband signal bandwidths for the sinusoidal test situation should be comparable to those under GMSK modulation.

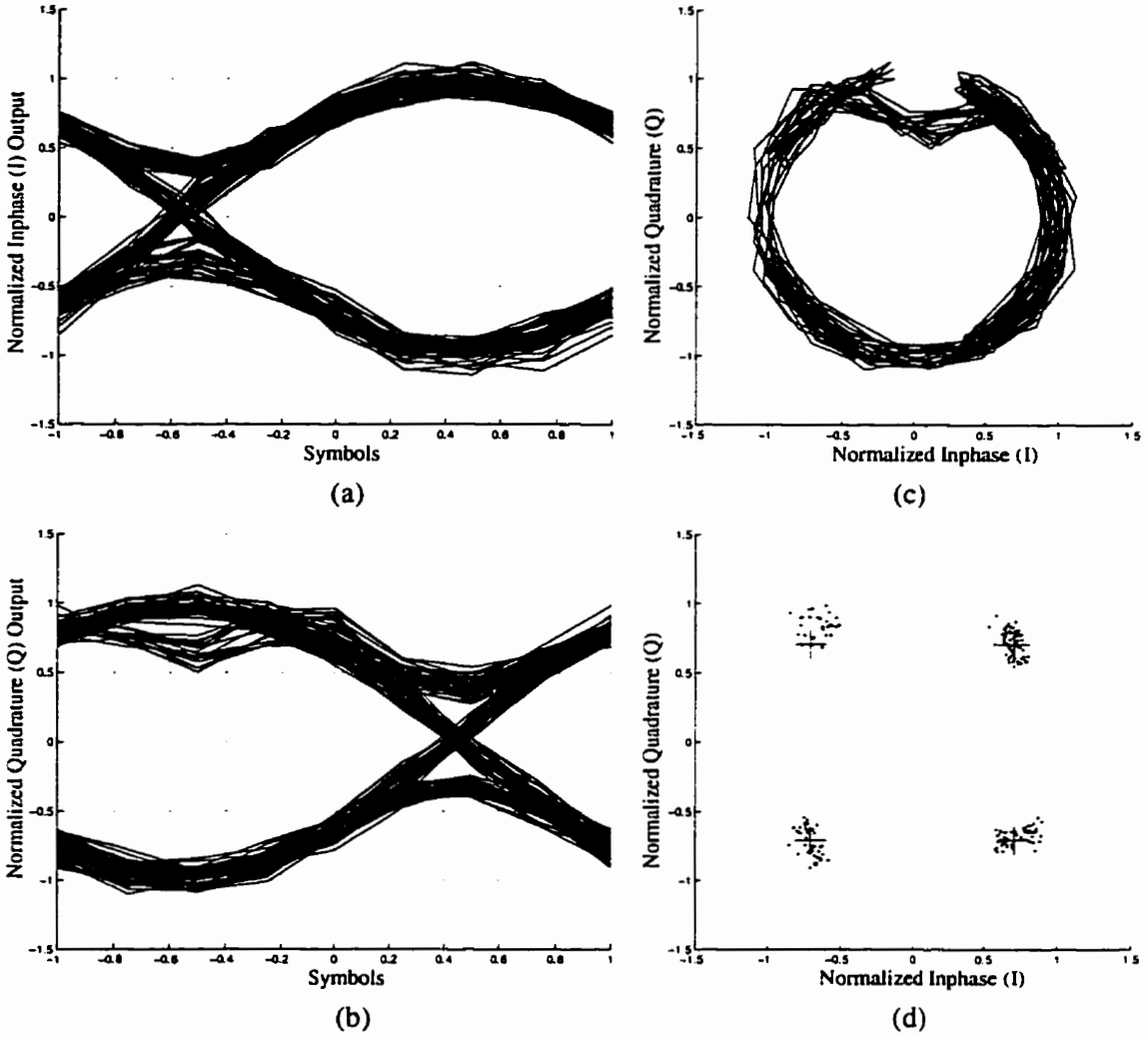


Figure 6.42 Coherent demodulation of 4 Mbps, 0.5 GMSK modulated carrier signal at 17.65 GHz: (a) Inphase Eye; (b) Quadrature Eye; (c) Vector; (d) Constellation.

Theoretically, a phase modulated signal has infinite bandwidth, although most appreciable modulated signal power is confined to a finite bandwidth about the carrier. For tone modulation with a modulating signal

$$m(t) = \alpha \cos \omega_m t, \tag{6.1}$$

the PM modulated carrier can be represented as

$$S_{PM}(t) = A \exp[\omega_c t + k_p \alpha \cos \omega_m t], \tag{6.2}$$

where $k_p \alpha \cos \omega_m t$ is the excess phase of the carrier and $k_p \alpha$ is the peak phase deviation. Since the modulator has a maximum phase control range of $\pm\pi$ over a voltage range of 14.1 V, $k_p = 0.22$ radians/volt, and the maximum value of $k_p \alpha$ is π. Equation 6.2 can be expanded using an exponential Fourier series and represented as a carrier component with an infinite number of sidebands as [20]

$$S_{PM}(t) = A \sum_{n=-\infty}^{\infty} J_n(k_p \alpha) \cos(\omega_c + n\omega_m)t, \tag{6.3}$$

where $J_n(k_p \alpha)$ is the nth order Bessel function of the first kind [50] representing the magnitude of the nth sideband at $\omega = \omega_c \pm n\omega_m$. The sideband levels relative to the carrier level (dBc) can be calculated as

$$P_n = 20 \log \left| \frac{J_n(k_p \alpha)}{J_0(k_p \alpha)} \right|. \tag{6.4}$$

It would be desirable to test the modulator using a sinusoidal modulating signal with a peak to peak amplitude spanning the entire 2π control voltage range. Unfortunately, Equation 6.4 suggests that with $k_p \alpha = \pi$, approximately 7 sidebands are required on each side of the carrier to accurately represent the modulated signal spectrum, before the sidebands fall to

negligible levels (ie:< -40 dBc). From Figure 6.23, the modulator output bandwidth at a carrier frequency of 17.65 GHz is expected to be on the order of 500 MHz. Therefore, the maximum modulation frequency is restricted to approximately $500/14 = 35$ MHz, over the full phase shift range.

In order to get a modulation signal which produced a modulated carrier spectrum more representative of GMSK, the amplitude was reduced until all but the first sideband on each side of the carrier was negligible. This provided a modulated signal bandwidth of $2f_m$, where f_m is the modulating tone frequency and is the condition of Narrowband FM (NBFM) [20]. This modulation condition is comparable to GMSK, where most of the modulating signal power is within a bandwidth of $1/T_b$ and the modulated signal power is within a bandwidth of $2/T_b$.

The sinusoidal modulating signal was chosen to have a peak to peak amplitude of 1 V, providing a peak phase deviation $k_p\alpha = 0.22$ radians and expected sideband levels of -19 dBc, as calculated using Equation 6.4. The modulating signal frequency was varied, while keeping the peak phase deviation in the modulator constant. Therefore, the relative levels of the sideband components should remain constant as the modulation frequency is increased.

Figure 6.43 shows the modulated signal spectrum at 17.65 GHz for various sinusoidal modulating frequencies. As seen from the figure, the sidelobes are quite well balanced around the carrier and within a couple of dB from ideal for modulating signal frequencies up to 300 MHz. Although not a direct test of the modulator bandwidth for GMSK modulation, this result is encouraging, and verifies the suitability of this modulator for high frequency CPM modulation, of which GMSK is one type.

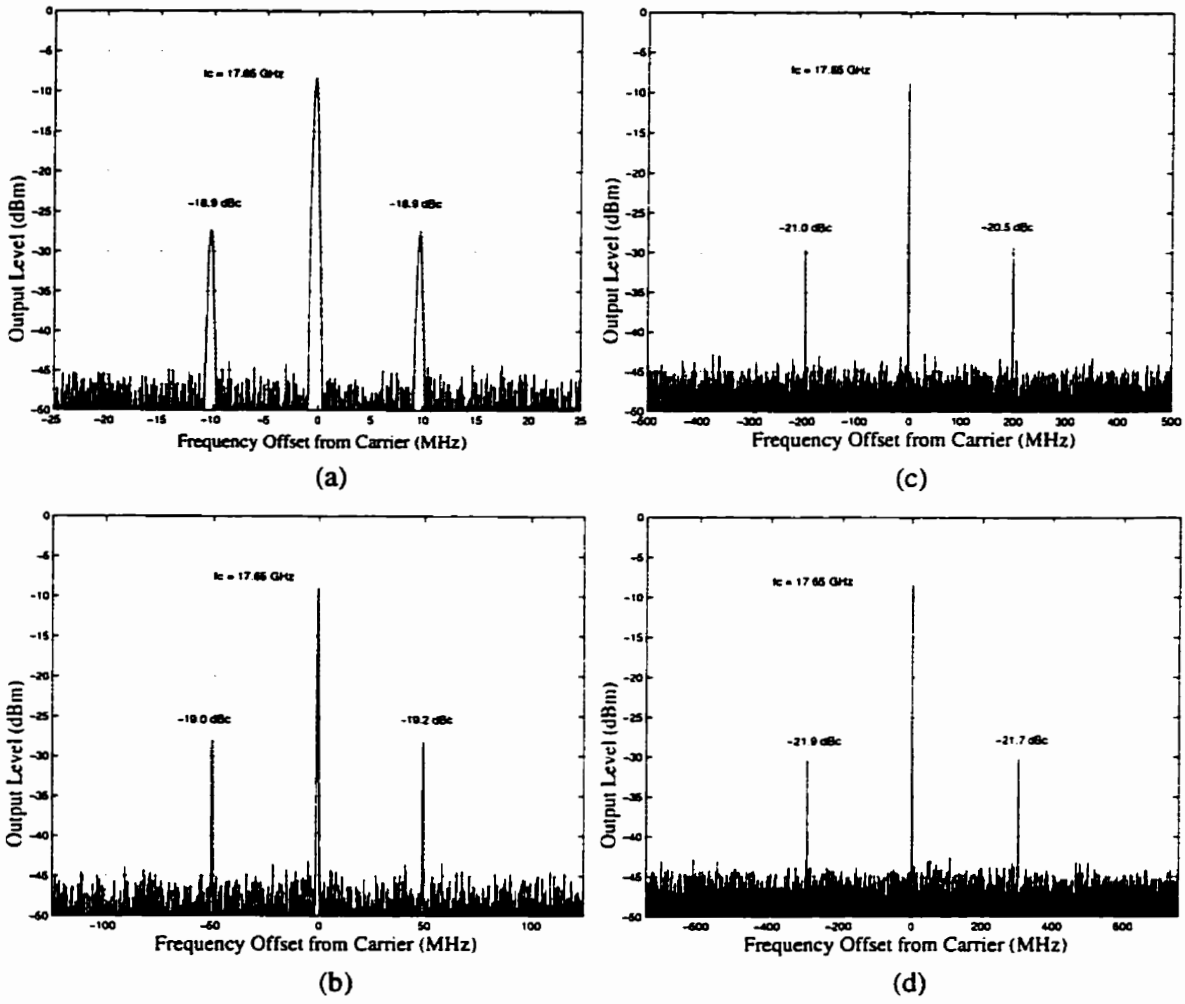


Figure 6.43 Sinusoidal phase modulated output signal spectrum at 17.65 GHz: (a) 10 MHz; (b) 50 MHz; (c) 200 MHz; (d) 300 MHz.

6.6 Suggestions for Improvements

Emphasis in this prototype modulator implementation was on verifying the feasibility of the proposed method of GMSK modulation at microwave frequencies. In order to optimize the modulator performance for a specific transmitter product, the following issues should be considered.

The fractional phase shifter performance presented in Section 6.3 was very close to that predicted by simulation, albeit slightly off frequency. The most significant cause of this difference can be attributed to variation in the termination varactor model parameters. No varactor models were available from the vendor, so the parameters for the varactor model shown in Figure 4.3 were estimated based on parameters available on the varactor datasheets. The basic varactor model used in Figure 4.3 appears sound, as the measured characteristics closely match the expected characteristics, but off frequency. Therefore, to get more predictable results at a specific frequency, more effort should be made in accurately predicting the varactor model parameters, either by obtaining more reliable vendor data or by characterizing a sample of available parts. The model could be improved by characterizing the varactor parasitic resistance as a function of bias, rather than keeping this parameter fixed. This would provide better prediction of the residual amplitude modulation characteristics of the phase shifter. The phase shifter could also be designed at a lower operating frequency, so that the varactor parasitic package capacitance became insignificant at low varactor capacitance values. This would make the phase shifter somewhat less sensitive to varactor parameter variation, but would require a higher multiplication factor in the frequency/phase multiplier to achieve the same modulated output frequency.

Limited tunability for MIC realizations could also be built into the fractional phase shifter terminations, which would make accurate characterization of the varactor parameters less critical. The easiest place to incorporate some tunability is in the short circuit microstrip lines. One possibility is a

sliding short circuit, realized by soldering a small gold tab between the termination microstrip lines and ground, at the appropriate place to change the electrical length and inductive reactance of the line.

The frequency/phase multiplier performance presented in Section 6.4 was also very close to that predicted by the simulations. Improving the multiplier performance as a hard-limiter would certainly be valuable, given that the input signals generally have some envelope variation. Cascaded stages of lower harmonic multipliers could be used to obtain strong FET saturation conditions, but this will increase the circuit complexity as a result of interstage filtering and matching requirements. A "saturation" condition based on the drain conduction angle as described in Section 4.2.2 could also be obtained in a high harmonic FET multiplier.

The coaxial to microstrip transitions also contributed to both the phase shifter and multiplier performance differences. Exact packaging details were not known or considered at the time of simulation. These transitions could easily be modelled and compensated for in the simulations to improve the input and output performance characteristics.

The suggestions for the phase shifter and multiplier would improve the overall performance of the modulator presented in Section 6.5. The effect of the inherent circuit lowpass characteristic on the $\pm\pi$ voltage discontinuity seems to be the major limiting factor on the modulator bandwidth. Design of high performance baseband circuitry as suggested in Section 6.5 should make high rate modulation feasible. If the baseband circuitry is implemented digitally, it is also straightforward to predistort the modulating signal at the $\pm\pi$ voltage discontinuity to compensate for the smoothing effects of the inherent circuit lowpass characteristic. This would extend the baseband bandwidth for GMSK modulation signals. Predistortion could also be used to improve the modulator phase shift linearity, if required, but the results of Section 6.5 suggest that this is likely unnecessary.

6.7 Summary

This chapter provided a detailed performance evaluation of the direct GMSK modulator MIC prototype. The performance of the fractional phase shifter and the frequency/phase multiplier circuits was evaluated separately, and the two circuits were combined in order to assess the overall modulator performance in providing GMSK modulation at 18 GHz. Some suggestions for improving the modulator were also discussed.

Both the fractional phase shifter and the frequency/phase multiplier performed exceptionally well and were comparable with the simulations of Chapter 5, although the optimal performance was slightly off of the simulation frequency. The optimal performance for the fractional phase shifter occurred at an operating frequency of 3.26 GHz, where a phase shift range of 72.2 degrees within 0.3 degrees from linear was observed. The operating frequency of 3.53 GHz was chosen for evaluation with the complete modulator. At 3.53 GHz, the phase shifter provided 72.6 degrees of phase shift range, while still maintaining very low phase error of 0.6 degrees. The frequency/phase multiplier effectively provided an output signal at $\times 5$ the input signal frequency, with a substantial output level of -10 dBm at 18 GHz. The frequency selectivity of the multiplier was also quite good as all undesired harmonics were maintained at < -30 dBc. The multiplier performance as a hard-limiter was not exceptional, as expected. The input to output level variation, however, was not much worse than linear and thus, did not contribute significantly to output level variation.

The overall modulator performed extremely well in effectively providing GMSK modulation at 18 GHz, with as little as 5 degree phase distortion in the modulated signal while maintaining the near constant envelope property for GMSK. The modulation performance at higher bit rates is degraded by the inherent circuit lowpass filtering effect on the $\pm\pi$ voltage discontinuity required in the modulating signal. This filtering effect seems to be a major

limiting factor on the modulator bandwidth, but does not necessarily inhibit coherent demodulation if maintained within acceptable levels. The filtering also results in a loss of the modulated signal constant envelope property, but this effect can likely be mitigated with better hard-limiting. This problem aside, the modulator was shown to be wideband to general CPM modulating signals, and performed quite well with modulating signal frequencies up to 300 MHz.

Although GMSK modulation was stressed in this research, the results suggest that this modulator architecture is an excellent general purpose microwave phase shifter/modulator useful for a variety of transceiver applications requiring linear 360 degree phase control of a carrier, including phase synchronization of antenna and oscillator arrays, phased array antenna beam steering, continuous phase modulation, indirect frequency modulation, and ultra-small carrier frequency translations.

7. CONCLUSIONS

This chapter summarizes the research presented in this thesis on the realization of direct GMSK modulation at microwave frequency. The motivation behind this research is revisited. The objectives of the research are discussed and satisfied based on the results presented. Based on the findings in this thesis, some conclusions are drawn, both on the results and on the significance of this work to future microwave and millimeter-wave radio systems. Further research directives are also suggested.

7.1 Summary

The motivation that drove this research arose from the current explosion in the demand for high speed wireless communication systems. These new and emerging systems are being forced into the upper microwave and millimeter-wave frequency bands as a result of congestion in the traditional microwave portions of the radio spectrum. At these frequencies, transceiver hardware architectures are less mature, and therefore, research into effective transmitter realizations suitable for use at these frequencies seemed very timely.

The features which make direct microwave modulation of a carrier signal attractive to effective transmitter designs were discussed. Continuous modulation of the phase of a microwave or millimeter-wave carrier signal over the full 360 degree range is an important fundamental requirement of direct modulation. In the design of wireless transmitters, effective realization of this principle is extremely valuable, as most modulation methods require encoding of baseband information in the phase of a carrier signal. It was suggested

that the ability to modulate the carrier phase directly, as opposed to the more traditional method of modulation at an IF frequency and use of multiple stages of upconversion to reach the desired transmit frequency, would make a simple and elegant hardware solution for a microwave transmitter feasible.

The Gaussian Minimum Shift Keying (GMSK) modulation method was discussed in detail. GMSK is one example of a modulation technique requiring full 360 degree phase control of the carrier signal, and was deemed appropriate for direct modulation. It was proposed that a method of direct GMSK modulation providing a frequency stable modulated output signal with simple and realizable hardware at microwave or millimeter-wave frequency would be very attractive for future high capacity radio systems.

The main objectives of the research were defined:

1. Devise a suitable hardware architecture for direct GMSK modulation at microwave frequency.

2. Implement the proposed hardware architecture using realistic microwave circuitry.

3. Evaluate the performance of the circuitry in realizing direct GMSK modulation at microwave frequency.

The first objective was satisfied after investigating some of the published methods for direct MSK and GMSK modulation. These methods, typically, were more appropriate for MSK than GMSK modulation, not appropriate for microwave frequency implementation, or resulted in complicated microwave hardware solutions. A novel hardware architecture resulting in an elegant hardware solution for direct GMSK modulation at microwave frequency based on a fractional range phase shifter and frequency/phase multiplier was proposed and patented. This architecture, incidentally, is also

appropriate for many other modulation or phase shifting applications requiring linear control of a carrier signal phase over the full 360 degrees range. For GMSK, the fractional range phase shifter operates as a CPFSK modulator at a subharmonic of the desired output signal frequency, with modulation index of $0.5/N$. The $\times N$ frequency/phase multiplier restores the modulation index to 0.5, while expanding the fractional phase shift range by a factor $\times N$ and multiplying the frequency by $\times N$.

Two methods of applying Gaussian filtering to the carrier signal phase were proposed. The first involved prefiltering the integrated baseband data and injecting this signal into the basic phase shifter/multiplier modulator. This low power signal could then be amplified using an efficient Class C amplifier, or used to phase lock or injection lock a power oscillator. The second method involved using the modulator to generate frequency stable MSK and using this signal as the reference signal for a high power phase locked oscillator, where a novel loop lowpass filter was proposed. The PLL loop characteristic with this lowpass filter provided Gaussian filtering to the carrier signal phase, as an option to prefiltering the baseband modulation signals.

The first method, that is, the basic phase shifter/multiplier modulator, was chosen to satisfy the second objective, namely designing realistic microwave hardware to realize GMSK modulation as proposed. The microwave circuitry was designed for an operating frequency of 18 GHz, with a subharmonic input CW reference signal of 3.6 GHz. This circuitry was exhaustively simulated using HP-EEsof Series IV© [43] microwave design software. A highly linear fractional range phase shifter based on a reflection topology, with reversed biased varactor diodes providing the reactive reflective terminations, was designed and simulated at 3.6 GHz. This circuit provided the required linear phase control range of $360/N$ degrees. A $\times 5$ frequency/phase multiplier consisting of a GaAs FET with strong Class C bias was designed

to provide useful 5th harmonic output level at 18 GHz with high rejection of unwanted harmonic components. The frequency/phase multiplier effectively expanded the linear phase control range in excess of 360 degrees, as confirmed by nonlinear circuit simulation. The encouraging simulation results proved that the modulator implementation was feasible.

After simulation, prototype modulator circuitry was designed using MIC technology with gold microstrip lines on an alumina substrate. The performance of the fractional phase shifter and the frequency/phase multiplier circuits was evaluated separately, and the two circuits were combined in order to assess the overall modulator performance in providing GMSK modulation at 18 GHz. Both the fractional phase shifter and the frequency/phase multiplier proved to be very high performance microwave circuits in their own right, with measurement results comparable to the simulations. The performance of the two circuits as a complete modulator was also tested using a variety of modulation signals to verify its functionality as a full 360 degree linear phase shifter, as well as a GMSK modulator. In all cases, the performance of the modulator was very good. The suitability of the modulator for high frequency modulation was also verified. The results of the testing confirmed that direct GMSK modulation was realized at microwave frequency using the proposed method, which was the third objective of the research.

7.2 Conclusions

The major conclusions of this work are summarized below.

1. An elegant hardware architecture for frequency stable, direct GMSK modulation of a microwave or millimeter-wave carrier signal has been realized. This architecture results in a simple microwave hardware solution, requiring only a single active device. The modulator was shown experimentally to provide effective GMSK modulation of a carrier signal at 18 GHz with Gaussian prefiltered control signals. The full GMSK excess phase trellis was

exercized with as little as 5 degree phase distortion in the modulated signal while maintaining the near constant envelope property desired for GMSK.

2. The GMSK modulation performance at higher bit rates is degraded by the inherent circuit lowpass filtering effect on the $\pm\pi$ voltage discontinuity required in the modulating signal to account for phase wrapping. This filtering effect is a limiting factor on the modulator bandwidth, and can likely be mitigated with better hard-limiting. This problem aside, the modulator was shown to be wideband in general, and performed well at modulation frequencies as high as 300 MHz.

3. The two main parts of the modulator, the fractional phase shifter and the frequency/phase multiplier, perform very well in their own right and are comparable to simulation. This fact lends much confidence to the process and the simulation tools used for the realization of this modulator implementation at 18 GHz. One could easily move with confidence in applying the principles presented in this thesis to higher frequency implementations. The fractional phase shifter provided a linear phase shift range of > 72 degrees with phase error typically of 0.5 degrees or less. The frequency/phase multiplier effectively provided an output signal at $\times 5$ the input signal frequency, with substantial output level and low levels of unwanted harmonics.

4. The modulator is a very useful circuit for much more than just GMSK modulation. In fact, many microwave circuit applications requiring full and accurate control of a carrier signal phase can be effectively realized using this modulator architecture. Examples of such applications include ultra-small carrier frequency translations, phase synchronization of antenna and oscillator arrays, phased array antenna beam steering, continuous phase modulation and indirect frequency modulation. It is also possible that this circuitry could be used to provide the phase control portion of linear modulation methods, employing combined amplitude and phase modulation of a carrier.

7.3 Significance

Several significant contributions to the field are evident from this work and have been recognized through several accepted papers and patents. These are summarized below.

1. The use of a nonlinearity to expand the linear phase shift range of a phase shifter/modulator is an excellent method of achieving a large range linear phase shifter with a very simple hardware solution. This is a very general principle that can be applied in a number of circuit applications requiring accurate and full range phase control of a microwave signal. It is also easy to expand the principle into higher millimeter-wave frequency bands by simply increasing the multiplier multiplication factor. To the Author's knowledge, this principle had not previously been exploited explicitly for this purpose.

2. A method of effectively matching the termination characteristics of a reflection phase shifter to the desired reactance tangent function, required for linear phase shifter operation, was developed. Hyperabrupt junction varactor diodes to compensate for the effects of parasitic varactor package capacitance were used, instead of abrupt junction varactors which are generally used for this application.

3. An effective $5th$ harmonic frequency multiplier was designed using a single GaAs MESFET. Previously published results suggested that multipliers of this type were practical only up to the $2nd$ or $3rd$ harmonic. Use of a single transistor stage is desirable, as it results in a much simpler hardware solution.

4. Use of the nonlinearity principle has resulted in a simple modulator architecture proven to work exceptionally well in effectively generating GMSK or other CPM modulations, at potentially high bit rates. This is a generic modulator structure that is appropriate for use at microwave or

millimeter-wave frequencies.

5. A new lowpass filter prototype has been developed for use with a phase locked power oscillator that applies Gaussian filtering to the phase of an MSK modulated carrier signal, as an alternative to baseband prefiltering. This principle could likely be extended to other filter characteristics in addition to Gaussian.

7.4 Future Research Directives

Future research is suggested in the following areas:

1. High speed digital baseband circuitry is required to realize a complete modulator using the method of digital generation and Gaussian prefiltering. The testing done to date synthesized control signals representative of random, Gaussian prefiltered data, but no testing with a high rate random serial bit stream has been done. Design of such circuitry is not trivial, if rates in excess of 20 Mbps are to be realized, remembering the oversampling requirements needed to synthesize appropriate analog phase control signals. This circuitry could be designed with provision for including predistortion to account for the circuit filtering effects at the $\pm\pi$ voltage discontinuity and extend the modulator bandwidth.

2. The principles used for the modulator realization at 18 GHz could be extended to other microwave or millimeter-wave bands, for emerging systems at these frequencies.

3. The usefulness of the modulator for realizing other microwave and millimeter-wave phase modulation and phase shifter functions should be explored.

4. The principles used in this research for prototype MIC circuit implementation could be extended to realize an MMIC implementation of the modulator circuits. This would potentially provide a single chip modulator

solution suitable for high volume transceiver applications. This extension would require, among other things, some additional work on realizing planar varactor equivalents suitable for MMIC realization.

5. Methods of using this modulator to effectively generate higher power modulated output signals as discussed in this thesis should be investigated, including phase locking or injection locking of high power oscillators and arrays.

6. This research has focused entirely on the transmitter. The other half of the wireless communications link is the demodulator. It is evident that based on the interest and significance of the research done on the modulator, that similar advances in effective demodulation structures at upper microwave and millimeter-wave frequencies can be achieved.

References

[1] A. J. Viterbi, "The Evolution of Digital Wireless Technology from Space Exploration to Personal Communication Services," *IEEE Transactions on Vehicular Technology*, Vol. 43, No. 3 , Aug. 1994, pp. 638-643.

[2] S. Kumar, A. Mohammadi, D. Klymyshyn, "Direct Microwave Frequency Modulation for a 155.52 Mbps 17.7 to 19.7 GHz Radio for ATM Traffic," *Asia-Pacific Microwave Conference*, Dec. 1996, pp. 1447-1550.

[3] A. Mohammadi, S. Kumar, D. Klymyshyn, "A 155.52 Mbps ATM Radio in 18 GHz Band using TCM-QAM," *Proceedings of the 8th International Conference on Wireless Communications*, Wireless '96, 1996, pp. 424-430.

[4] H. H. Meinel, "Commercial Applications of Millimeterwaves History, Present Status, and Future Trends," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 43, No. 7, July 1995, pp. 1639-1653.

[5] K. Murota, K. Hirade, "GMSK Modulation for Digital Mobile Radio Telephony," *IEEE Transactions on Communications*, Vol. COM-29, No. 7, July 1981, pp. 1044-1050.

[6] K. Feher, H. Mehdi, "Modulation/Microwave Integrated Digital Wireless Developments," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 43, No. 7, July 1995, pp. 1715-1731.

[7] S. Kumar, "Directly Modulated VSAT Transmitters," *Microwave Journal*, Vol. 33, No. 4, April 1990, pp. 255-264.

[8] D. M. Klymyshyn, "A Power Amplifier Linearizer using Adaptive Poly-

nomial Predistortion," M.Sc. Thesis, Dept. of Electrical Engineering, University of Saskatchewan, August 1995.

[9] P. Varshney, S. Kumar, J. E. Salt, "Performance of GMSK with Two-Bit Differential Detection in a Land Mobile Radio Channel," *Can. J. Elect. & Comp. Eng.*, Vol. 19, No. 1, 1994, pp. 37-43.

[10] M. K. Simon, C. C. Wang, "Differential Detection of Gaussian MSK in a Mobile Radio Environment," *IEEE Transactions on Vehicular Technology*, Vol. 33, No. 4, Nov. 1984, pp. 307-320.

[11] J. B. Anderson, C-E. W. Sundberg, "Advances in Constant Envelope Coded Modulation," *IEEE Communications Magazine*, Dec. 1991, pp. 36-45.

[12] D. R. Smith, *Digital Transmission Systems*, USA, Van Nostrand Reinhold Co., 1985.

[13] R. E. Ziemer, C. R. Ryan, "Minimum-Shift Keyed Modem Implementations for High Data Rates," *IEEE Communications Magazine*, Vol. 21, Oct. 1983, pp. 28-37.

[14] J. G. Proakis, *Digital Communications*, USA, McGraw-Hill, 1989.

[15] S. Benedetto, E. Biglieri, V. Castellani, *Digital Transmission Theory*, USA, Prentice-Hall, 1987.

[16] K. Feher, *Advanced Digital Communications - Systems and Signal Processing Techniques*, USA, Prentice-Hall, 1987.

[17] S. Ariyavisitakul, T. P. Liu, "Characterizing the Effects of Nonlinear Amplifiers on Linear Modulation for Digital Portable Radio Communications," *IEEE Transactions on Vehicular Technology*, Vol. 39, No. 4 , Nov. 1990, pp. 383-389.

[18] A. I. Zverev, *Handbook of Filter Synthesis*, New York, USA, John Wiley & Sons, 1967.

[19] J. Smith, *Modern Communication Circuits*, USA, McGraw-Hill, 1986.

[20] B.P. Lathi, *Modern Digital and Analog Communication Systems*, USA, Holt, Rinehart and Winston, Inc., 1989.

[21] R. V. Garver, "360° Varactor Linear Phase Modulator," *IEEE Transactions on Microwave Theory and Techniques*, Vol. MTT-17, No. 3, March 1969, pp. 137-147.

[22] S. Lucyszyn, I. D. Robertson, "Analog Reflection Topology Building Blocks for Adaptive Microwave Signal Processing Applications," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 43, No. 3, March 1995, pp. 601-611.

[23] F. Ali, N. Mysoor, "An Analog MMIC Phase Modulator for X-Band Satellite Transponder Applications," *IEEE Microwave and Guided Wave Letters*, Vol. 2, No. 11, Nov. 1992, pp. 445-446.

[24] S. Lucyszyn, I. D. Robertson, H. Aghvami, "24 GHz Serrodyne Frequency Translator using a 360° Analog CPW MMIC Phase Shifter," *IEEE Microwave and Guided Wave Letters*, Vol. 4, No. 3, March 1994, pp. 71-73.

[25] X. Zhang, A. S. Daryoush, "Full 360° Phase Shifting of Injection Locked Oscillators," *IEEE Microwave and Guided Wave Letters*, Vol. 3, No. 1, Jan. 1993, pp. 14-16.

[26] D. M. Klymyshyn, S. Kumar, A. Mohammadi, "A 360° Linear Microwave Phase Shifter with a FET Frequency/phase Multiplier," *Microwave Journal*, Vol. 40, No. 7, pp. 130-137, July 1997.

[27] D. M. Klymyshyn, S. Kumar, A. Mohammadi, "Microwave Phase Shifter," Canadian and U.S. Patents Pending.

[28] D. M. Klymyshyn, S. Kumar, A. Mohammadi, "Linear Reflection Phase Shifter with Optimised Varactor Gamma," *Electronics Letters*, Vol. 33, No. 12, pp. 1054-1055, June 1997.

[29] D. M. Klymyshyn, S. Kumar, A. Mohammadi, "Frequency Stabilized Direct GMSK Modulator," *Ninth IEEE International Symposium on Personal, Indoor and Mobile Radio Communications*, Sept. 1998, and also under review by *IEEE Transactions on Vehicular Technology.*

[30] D. M. Klymyshyn, S. Kumar, A. Mohammadi, "GMSK Modulator Formed of PLL to Which Continuous Phase Modulated Signal is Applied," Canadian and U.S. Patents Approved, April 1998.

[31] J. Klapper, J. Frankle, *Phase-Locked and Frequency-Feedback Systems*, New York, USA, Academic Press Inc., 1972.

[32] I. D. Robertson (Editor), *MMIC Design*, London, UK, Institution of Electrical Engineers, 1995.

[33] D. M. Pozar, *Microwave Engineering*, USA, Addison-Wesley, 1990.

[34] Alpha Industries Databook, *Semiconductors and MMICs - Products for Wireless and Commercial Applications*, Woburn MA, USA, Alpha Industries Inc., 1996.

[35] W. A. Davis, *Microwave Semiconductor Circuit Design*, USA, Van Nostrand Reinhold Co., 1984.

[36] S. A. Maas, *Nonlinear Microwave Circuits*, Norwood, MA, USA, Artech House, Inc., 1988.

[37] A. Gopinath, J. B. Rankin, "Single-Gate MESFET Frequency Doublers," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 30, No. 6, June 1982, pp. 869-875.

[38] C. Rauscher, "High-Frequency Doubler Operation of GaAs Field-Effect Transistors," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 31, No. 6, June 1983, pp. 462-473.

[39] G. S. Dow, L. S. Rosenheck, "A New Approach for mm-Wave Generation," *Microwave Journal*, Vol. 26, No. 9, Sept. 1983, pp. 147-162.

[40] K. Shirakawa, Y. Kawasaki, Y. Ohashi, N. Okubo, "A 15/60 GHz One-Stage MMIC Frequency Quadrupler," *Proceedings of the IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium*, 1996, pp. 35-38.

[41] M. Cohn, R. G. Freitag, H. G. Henry, J. E. Degenford, D. A. Blackwell, "A 94 GHz MMIC Tripler using Anti-Parallel Diode Arrays for Idler Separation," *Proceedings of the IEEE MTT-S International Microwave Symposium*, 1994, pp. 763-766.

[42] F. Brauchler, J. Papapolymerou, J. East, L. Katehi, "W Band Monolithic Multipliers," *Proceedings of the IEEE MTT-S International Microwave Symposium*, 1997, pp. 1225-1228.

[43] HP EEsof Series IV Manuals, *HP EEsof High-Frequency Design Solutions*, USA, Hewlett-Packard Co., Release 6.0, July 1995.

[44] R. H. Hoffmann, *Handbook of Microwave Integrated Circuits*, USA, Artech House Inc., 1987.

[45] T. Laverghetta, *Microwave Materials and Fabrication Techniques*, USA, Artech House Inc., 1991.

[46] M/A-Com Databook, *RF and Microwave Semiconductors - Diodes, Transistors and Integrated Circuits*, Burlington, MA, USA, M/A-Com Inc., 1994.

[47] I. Bahl, P. Bhartia, *Microwave Solid State Circuit Design*, USA, John Wiley & Sons, 1988.

[48] R. W. Rhea, *HF Filter Design and Computer Simulation*, USA, McGraw-Hill, 1995.

[49] G. Gonzalez, *Microwave Transistor Amplifiers - Analysis and Design*, USA, Prentice-Hall, 1997.

[50] C. R. Wylie, *Advanced Engineering Mathematics*, USA, McGraw-Hill, 1975.